INTEGRATED RETINAL IMPLANTS

Thesis by

Wen Li

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To my family

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ABSTRACT

Integrated wireless implants have always been the ultimate goal for neural prostheses. However, technologies are still in development and few have actually been transferred to clinical practice due to constraints in material biocompatibility, device miniaturization and flexibility. In this dissertation, emphasis is placed on the development of Parylene devices for neural prostheses, and particularly, for retinal prostheses that partially restore lost vision for patients suffering from outer retina degeneration.

A basic Parylene-metal-Parylene skin technology for making planar Parylene micro-electro-mechanical systems (MEMS) devices, such as electrode arrays and radio-frequency (RF) coil, is first discussed, followed by accelerated lifetime soaking tests to investigate the long term stability of such skins in hot saline under both passive and active electrical stressing. Discussion is further expanded on a detailed description of the design, fabrication, and testing procedure of two types of MEMS coils, which serve as receiver coils for wireless power and data transfer in a retinal implant system. After that, an embedded chip integration technology is presented, which allows the integration of complementary metal-oxide-semiconductor (CMOS) integrated circuit (IC) chips with other MEMS devices and discrete components so as to achieve high-level system functionality. Finally, an integrated wireless neural stimulator is designed and successfully fabricated using a test chip.

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NOMENCLATURE

MEMS: Micro-electro-mechanical systems

RF: Radio-frequency

CMOS: Complementary metal-oxide-semiconductor

IC: Integrated circuit

AMD: Age-related macular degeneration

RP: Retinitis pigmentosa

WHO: World Health Organization

USC: University of Southern California

MST: Microsystems technology

DRIE: Deep reactive-ion etching

LIGA: German acronym for “X-ray lithography, electroforming, and molding”

HNA: Hydrofluoric acid & Nitric acid & Acetic acid

TAMH: Tetra-methyl-ammonium-hydroxide

PDMS: Poly(dimethylsiloxane)

USP: United States Pharmacopeia

ASIC: Application-specific integrated circuit

ALST: Accelerated-lifetime soaking test

RIE: Reactive ion etch

MTTF: Mean-time-to-failure

WVTR: Water vapor transmission rate

WVP: Water vapor permeability

SEM: Scanning electron microscopy

EDS: Energy dispersive X-ray spectroscopy

SAR: Specific absorption rate

ESR: Effective series resistance

UCSC: University of California, at Santa Cruz

MFI: MicroFlex interconnection

CL-I^2: Chip-level integrated interconnect

RFID: Radio-frequency identity

TTL: Transistor-transistor logic

ACIOL: Chamber intraocular lens

HMDS: Hexamethyldisilazane

BHF: Buffered hydrofluoric acid

IPA: Isopropanol

Chapter 1 INTRODUCTION

1.1 Outer retinal diseases

Age related macular degeneration (AMD) and retinitis pigmentosa (RP) are two of the most common outer retinal degenerative diseases that result in human vision impairment and blindness. According to the World Health Organization (WHO), AMD has become the third leading cause of blindness on global scale, and ranks first in developed countries [1]. In fact, it has been estimated that almost 3 million people in the United States will have significant symptoms associated with AMD by 2020 [2]. As for RP, it has affected more than 500,000 people in the United States, among whom 20,000 are legally blind [3]. AMD primarily affects the central vision regions in people age 60 and older (Figure 1.1 (b)). Because the brain will compensate for central dark patches during its early stages, it is difficult to diagnose this disease until the advanced stages. Whereas for patients with RP, vision deterioration develops gradually and progressively, starting from defective dark adaptation (night blindness), followed by the reduction of peripheral vision (known as tunnel vision in Figure 1.1 (c)), and, sometimes, a complete vision loss in the advanced stages of the disease [4].

Figure 1.1: (a) Normal vision. (b) Loss of central vision in patients with AMD. (c) Tunnel vision in patients with RP. (Images courtesy of Artificial Retina Project)

Although the mechanisms of these retinal diseases are not fully understood, histopathological studies indicate they are mainly restricted to outer retinal region, and associated with the damage of photoreceptor cells [5-8]. The photoreceptor cells (rods and cones) are situated in a deep retinal layer, and they, along with other cells (bipolar, ganglion, horizontal and amacrine cells), perform significant visual processing and communication tasks in normal vision (Figure 1.2). In a healthy retina, particularly, the photoreceptors initiate neural responses to incoming light by converting light into chemical and electrical signals. The bipolar and ganglion cells in the inner retina then pass the visual signals toward the optic nerve. Along the way, the horizontal and amacrine cells provide lateral interaction between neighboring cells [9].

Current treatments for such retinal degenerative diseases rely on gene replacement therapy, pharmaceutical therapy, nutritional therapy and dietary to slow down the development of blindness in their early stages [10, 11]. Nevertheless, once the vision is completely lost, no effective treatment exists that can cure these diseases. Studies on animal models show that photoreceptor and stem cell transplantations could be possible treatments by replacing the damaged retinal cells [12, 13]. However, they are still in

development, and not yet ready for clinical practice. Other concerns such as expensive costs and political issues also add barriers to their implementation. An alternative approach is proposed as bioelectronic visual prostheses, which bypass the damaged photoreceptor cells and utilize electrical stimulating to restore vision.

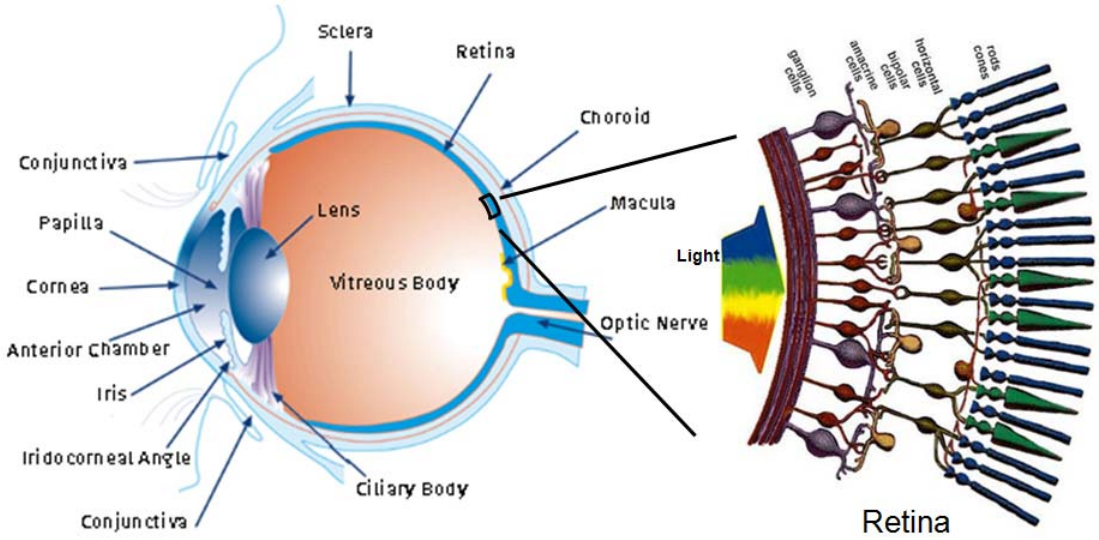


Figure 1.2: Horizontal cross section through human eye and the cell layers in the retina. (Eye illustrate adapted from Bausch & Lomb)

1.2 Artificial visual prostheses for AMD and RP treatments

1.2.1 Introduction to visual prostheses

Efforts to develop neural prostheses are not new. In fact, intensive studies have been done since the 18th century, using electronic devices to stimulate neurons and muscles for the control of limbs and organs, or to elicit sensory sensation for feeling, hearing or seeing. For instance, cochlea implants and pacemakers, the best-known neural prostheses, have been accepted in clinical practice in recent decades (Figure 1.3). For visual prostheses, investigations on implantation devices began from the 1960's. Since then,

many different approaches have been developed to restore lost vision function for blind patients, and each of them has distinct advantages and disadvantages.

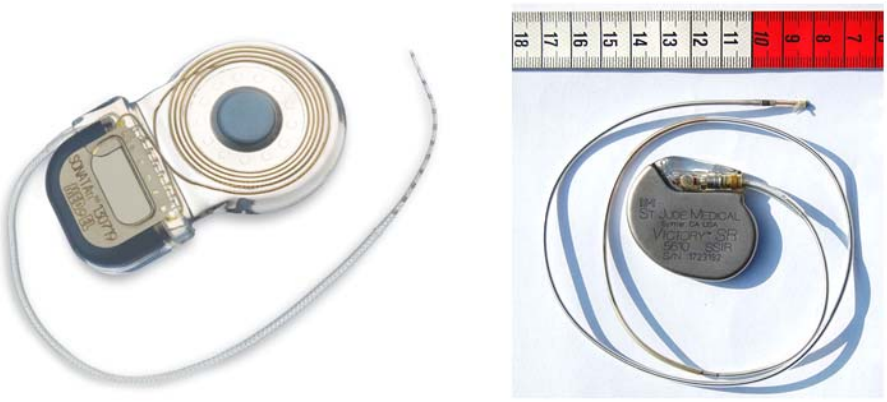


Figure 1.3: Two commercially available neural prosthesis products: (a) A single channel cochlear implant (Image adapted from Med-EL medical electronics). (b) A single channel pacemaker. (Image adapted from Wikimedia Commons)

I. Visual cortex prosthesis

Early work toward visual prostheses started from electrical stimulation of visual cortex. In 1968, Brindley and Lewin implanted 80 platinum electrodes on the visual cortex of a 52-year-old blind patient though a burr hole [14]. They found that when excited by appropriate radio signals, the patient could experience sensations of light (phosphenes). Inspired by this work, Dobelle and Mladejovsky continued their investigation on 37 human subjects [15]. In 2000, Dobelle reported a subject who had been wearing a cortical visual prosthesis system for over 20 years [16]. This result demonstrated the clinical feasibility and stability of such cortical prosthesis system for the long-term implantation (Figure 1.4). However, the early studies used large electrodes and thus had drawbacks including flickering phosphene, interactions between phosphenes, limited resolution, pain, local

heating and electrolysis [9]. To overcome these problems, modifications to the implant systems, such as the development of microelectrode arrays (Figure 1.5), have been made in recent years. These modifications enabled devices to be embedded in the visual cortex (intracortical implants) and therefore higher resolution and lower stimulation current could be achieved.

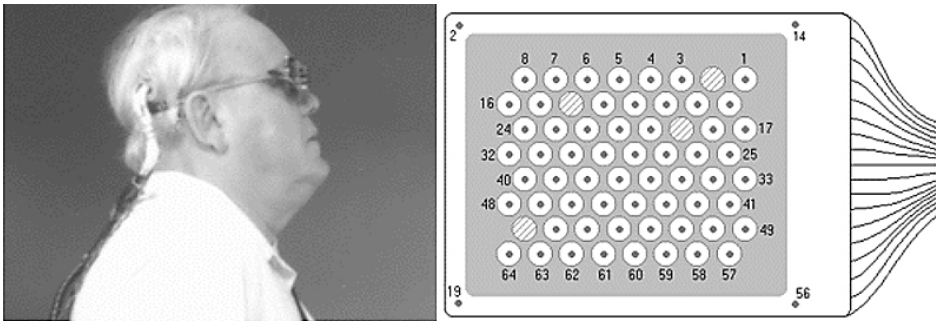
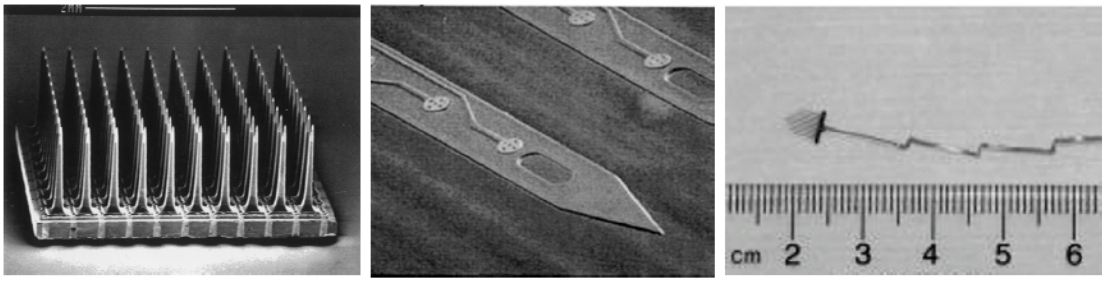


Figure 1.4: A blind patient with a cortical prosthesis system for over 20 years. The right picture shows the implanted 64-electrode array. The wires are connected to electrodes through a burr hole.



(a) (b) (c)

Figure 1.5: Several types of microelectrodes for cortical prostheses: (a) Utah 100-channel electrode array [17]. (b) Michigan 16-channel electrode array with flexible silicon ribbon cable [18]. (c) Caltech 2-D 32-channel electrode array with flexible Parylene cable [19].

The main advantage of the cortical stimulation approach is that the skull can provide good protections for implanted devices. In addition, the technique bypasses diseases proximal to the primary visual cortex, making it potentially useful for treating the largest number of blind patients suffering from both optic nerve and retina damages.

However, this technique has inevitable disadvantages. First of all, spatial organization is more complicated at the cortical level and two adjacent stimulation sites are not necessarily located at adjacent areas in space, so that patterned electrical stimulations may not produce the same perceptional patterns. Additionally, the surgical procedure is difficult and complicated, which can have devastating results, including death. Finally, local heating is still a problem due to poor heat dissipation inside the brain.

II. Optic nerve prosthesis

Optic nerve prosthesis uses direct optic nerve stimulation to restore vision. In one method, spiral cuff electrodes were placed around the optic nerve of blind patients (Figure 1.6 (a)). Electrical stimulus applied to the optic nerve produced localized, sometimes colored phosphenes throughout the visual field. By varying the duration and amplitude of the stimulus, patients were able to perceive different brightness of phosphene [20]. Another method called "hybrid retinal implant" was conducted in recent years [21], which involves culturing neurons on micro-electro-mechanical systems (MEMS). MEMS components were connected with the central nervous systems (CNS) though cultured neurons and their extended axons. By this means, electrical stimulation from the electrodes will excite the cultured neurons to send action potentials toward the CNS neurons, and thus restore vision.

Optic nerve prostheses can potentially be useful for both retinal degenerative and non-retinal degenerative blindness, without requiring surgical penetration of sensitive intracranial tissues. However, there are major problems associated with this approach: difficulties with high density stimulation and detail perception due to the high density of

the axons; surgical complexity and possible harmful side effects after implantation; and finally the difficulty to implement a complete intraocular system.

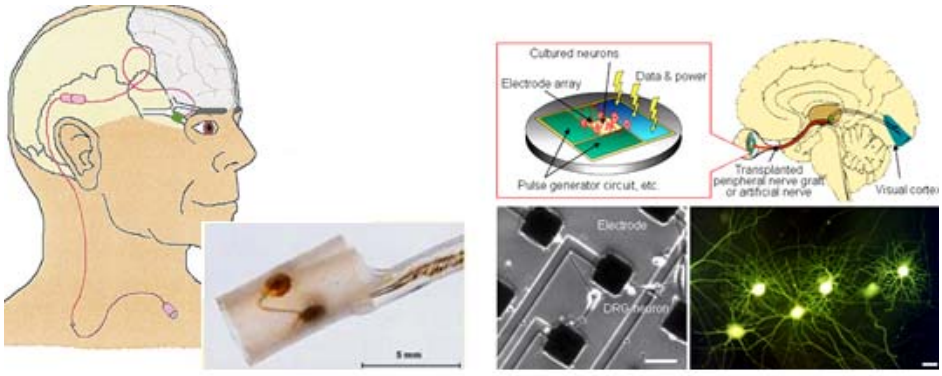


Figure 1.6: Optical nerve prosthesis systems: (a) Approach used spiral cuff electrodes [20]. (b) "Hybrid retinal implant" approach [21].

III. Retinal prosthesis

The retinal prosthesis approach aims to use the remaining visual pathway component (optic nerve bipolar and ganglion cells) to provide partial restoration of vision. In the 1990's, Humayun et al. conducted morphometric analysis of the retina of RP patients. They discovered that although the retinal photoreceptors are defective in those patients, their optic nerve, bipolar and ganglion cells to which the photoreceptors synapse remain functioning at a large rate [22]. Further studies showed similar results in AMD patients [23]. These results created profound impact on the ophthalmology field, by providing the possibility of using retinal prostheses to treat AMD and RP patients. Two types of prostheses are currently in development according to the layer of retina receiving the implanted device: subretinal and epiretinal.

The subretinal prosthesis is performed behind the retina between the bipolar cell layer and the retinal pigment epithelium, by replacing the degenerated photoreceptors with

electronic devices (Figure 1.7). Microfabricated photodiodes are implanted either in the subretinal space through an incision in the sclera or by standard vitrectomy followed by retinotomy. The microphotodiodes are stimulated by incident light through the retina, and the resulting electric current excites adjacent sensory neurons. Because the devices are placed closer to the bipolar cells, small stimulation currents (50 μA) were reported to be sufficient to excite the neuron cells [24]. Clinical trials have been done by implanting arrays with 5000 microphotodiodes into right eyes of 6 patients with RP [25]. Visual function improvement occurred in all subjects, with no significant safety-related adverse effects (implant rejection, infection, retinal detachment, etc.) being observed after up to 18 months. This result demonstrates the safeness and efficacy of such subretinal prosthesis approach in short- term implantation.

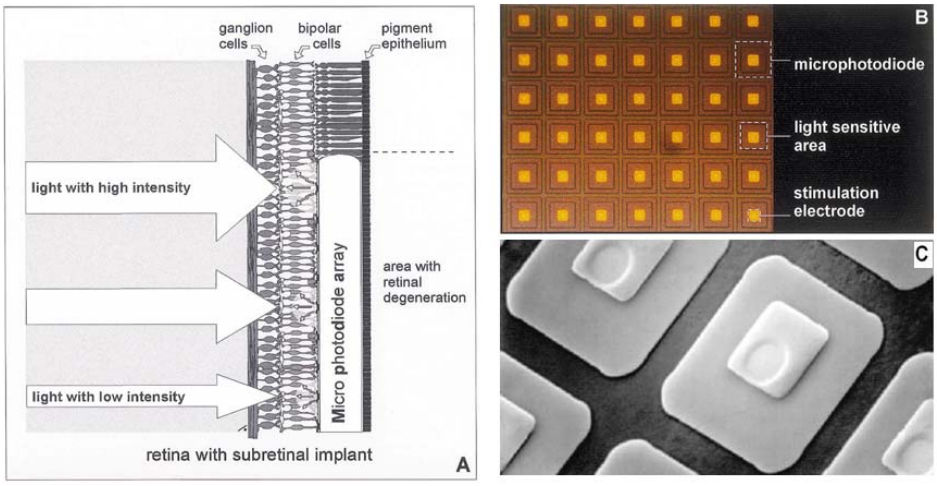


Figure 1.7: Subretinal prostheses. (a) Schematic showing the location of the implants. (b) The microphotodiode array made by Zrenner et al [24]. (c) The 5000 microphotodiode array made by Chow et al [25].

Although the subretinal prosthesis shows advantages including lower stimulus threshold, high–density stimulation, and perhaps better heat dissipation through choroid,

there are still many problems with the current implant system. The main disadvantage is the disruption to the nutritional supply of the retina derived from the choroid due to the introduced barrier between the outer retina and the choroid. In addition, only a small amount of light can reach the microphotodiodes through retina, and therefore the efficiency of the system is dramatically reduced. The long-term stability of the subretinal prosthesis has not yet been verified, which is also a big concern for its final implementation.

An epiretinal prosthesis system usually employs a multielectrode array implanted on the surface of the inner retina between the vitreous and internal limiting membrane. A data acquisition system located outside of the body captures images from the surroundings, and converts the information into patterns of electrical signals. Upon the reception of signals through data transmission and processing systems, the electrodes stimulate the remaining retinal ganglion cells and restore vision (Figure 1.8).

A major concern with epiretinal implantation is that the implants will be exposed to ocular rotational movements, raising the need for a reliable attachment method to fix the electrode array on the retina. Despite this drawback, we believe epiretinal implantation is the most promising technology for treating AMD and RP diseases among all visual prosthesis approaches, because of its many advantages compared to others. First, the epiretinal implantation and follow-up examination only require standard ophthalmologic technologies, reducing the risk of trauma during the surgery as well as allowing for the implant to be replaced. In addition, most of the implanted electronics is kept in the vitreous cavity, such that the implant can take the advantage of the heat dissipating properties of the vitreous, and thus causes less damage to the retina compared with subretinal implants.

Developments of MEMS technologies provide the possibility of complete intraocular retinal implants and high-density array stimulation.

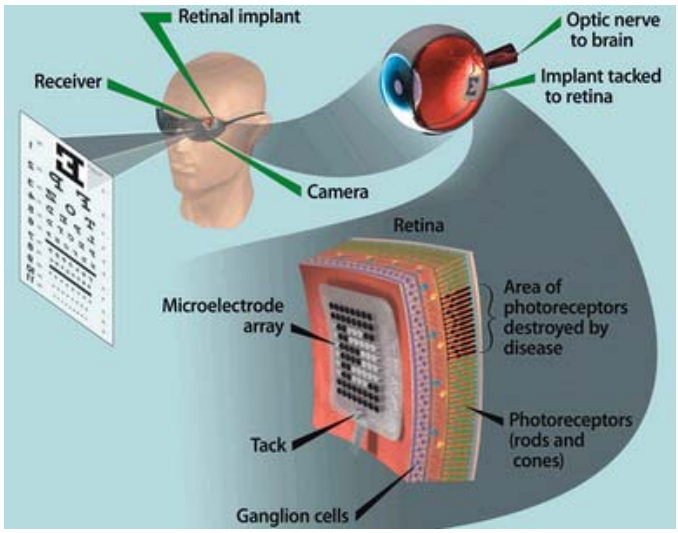


Figure 1.8: System overview of the epiretinal prosthesis. (Illustration courtesy of NextGenLog)

1.2.2 **State-of-the-art for epiretinal prostheses**

In 1994, Humayun et al. reported the results of electrically stimulating vertebrate retinas, showing that surface electrical stimulation of the inner retina in eyes with outer retinal degeneration can elicit a localized retinal response [26]. Since then, his team at the Doheny Eye Institute at the University of Southern California (USC), collaborating with a group of researchers, has developed an extraocular retinal prosthesis technology. The implanted unit of the first generation model consists of an intraocular part (electrode array) and an extraocular part (electronic box including a receiving coil). A 16 platinum microelectrode array, made by Second Sight Medical Products, Inc (Sylmar, CA, USA), is positioned temporal to the fovea and is attached to the inner retinal surface using a single tack. A hand-made coil is implanted outside of the eye, in the temporal skull to transfer

power and data through a telemetry link. After demonstrating the device functionality in animal models and short-term human studies, clinical trials of the IRP was conducted in 2002 to verify the chronic, long-term feasibility of the implants. To date, 6 patients with bare light perception have received the implants. Current results show that subjects can distinguish motion and locate objects (plate, cup, and knife). They have also shown the ability to discriminate between percepts created by different electrodes based on their locations [27]. Another clinical trial of an epiretinal implant, featuring a stimulation array of 49 platinum electrodes on a polyimide substrate, has recently been performed by Intelligent Medical Implants AG (Zurich, Switzerland). Subjects with implants can see phosphenes and crude shapes correlating to applied stimuli [28].

Several other groups worldwide have developed different designs of epiretinal implants that vary in terms of system configurations. All these implants are guided by similar requirements, including preserving as much of the normal visual function as possible while minimizing the amount of implanted electronics. Their functionality and short-term stability have been confirmed in both animal models and human subjects. However, clinical trials are still needed to demonstrate the long-term performances of implants.

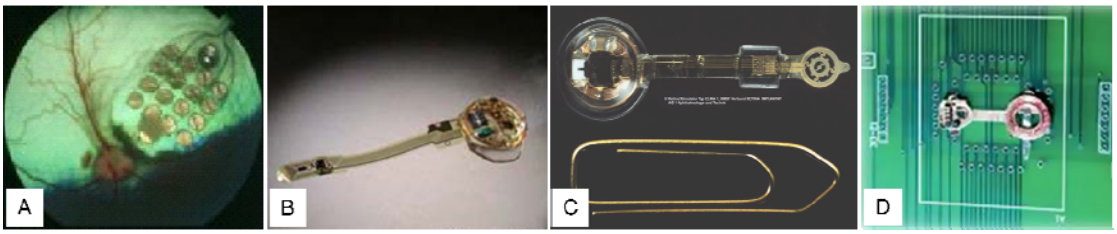


Figure 1.9: Several epiretinal implants: (a) Implanted Second Sight 16 electrode array [27]. (b) Retinal stimulator developed by Intelligent Medical Implants (Image adapted from Intelligent Medical Implants). (c) Epiretinal stimulator made by the German team.

(d) Test platform of an epiretinal prosthesis system (Rizzo and Wyatt) (Image adapted from The Boston Retinal Implant Project).

1.2.3 **Technical challenges of advanced epiretinal prostheses**

The next generation epiretinal prosthesis will require entirely intraocular implants to minimize surgical complexity as well as to reduce physical damages to patients during implantation. In this case, a receiving coil of the telemetry link, along with electronic circuitry, will be placed inside the eye in the anterior chamber or lens capsule. A flexible cable extends through the posterior chamber to reach the multielectrodes array attached on the inner retina surface. Due to the limited space of the human eye (< 1 cm^3), miniaturization is demanded for such an implant system. MEMS technology, as described in the next section, is a great candidate.

Most of the designs for intraocular retinal prostheses so far have been focusing on discrete devices, then using hand assembly for the system integration. However, a larger number of electrodes will be needed for advanced retinal prostheses to provide more information at higher spatial resolution in order to improve the quality of the image. A conservative estimate of pixel density will be 32×32 to enable blind individuals to better carry out activities of daily living [28]. Current interconnect and packaging technologies are labor-intensive, inefficient, and costly, limiting the achievable device resolution. A desired approach would be to build microfabricated devices in a process compatible way, while still sufficiently versatile to integrate other discrete components (application specific integrated circuits (ASICs), capacitors, etc.).

Furthermore, retinal implants will need to address the long-term biocompatibility issue of the electronics and the multielectrode array in the saline environment of human eyes. Thus a hermetic, biocompatible, flexible packaging technology will be necessary to protect such implanted components from the corrosive substances. To overcome this challenge, Parylene C is selected as the main structural and packaging material because of its many favorable properties which will be discussed in the next section.

1.3 Parylene-based MEMS technologies

1.3.1 Introduction to MEMS

MEMS, also called micromachines (in Japan) or microsystems technology (MST) (in Europe), is a microfabricated system comprising both electrical and mechanical components. Typical dimensions of such systems range from 100 nm to millimeters. The beginning of MEMS field concurred with the invention of the transistor by John Bardeen and Walter Brattain in 1947. In 1959, Richard Feynman mapped out the tremendous potentialities for miniaturization of machines to the scientist community, in his famous talked titled "There's plenty of room at the bottom." Since then, much attention has been drawn to this field, and a wide variety of MEMS devices have been built, such as micro-motor [29] and accelerometer [30].

In addition to the device and application development, processing technologies and materials used in MEMS are continually evolving. From the processing aspects, many basic MEMS techniques are borrowed or adapted from semiconductor fabrication, such as photolithography, oxidation, physical vapor deposition, chemical vapor deposition, dry plasma etching. Other techniques specifically for MEMS have also been developed, such

as deep reactive-ion etching (DRIE), LIGA (German acronym for "X-ray lithography, electroforming, and molding"), electroplating, and soft lithography. From the material aspects, alternative substrate, such as glass and polymers are introduced. The driving factor for this change is the demand for making devices that are more biocompatible and cheaper. In fact, after polymer materials were introduced a few decades ago, MEMS has become a key technology for interfacing integrated electronics and living cells for biomedical applications [31].

In order to build complicated devices for various applications, multiple basic process steps are combined in two general ways: bulk micromachining and surface micromachining [32]. Bulk micromachining, as illustrated in Figure 1.10-A, uses chemical etching or plasma etching to selectively remove substrate material with oxide or photoresist as masking films. Typical etching process can be either isotropic etching using HNA (hydrofluoric acid + nitric acid + acetic acid) and XeF_2, or anisotropic etching using KOH, TMAH (tetra-methyl-ammonium-hydroxide) and plasma. Among these techniques, DRIE, particularly the Bosch process, is developed for creating very high-aspect ratio structures, and even vertical through trenches in substrates (Figure 1.10-B).

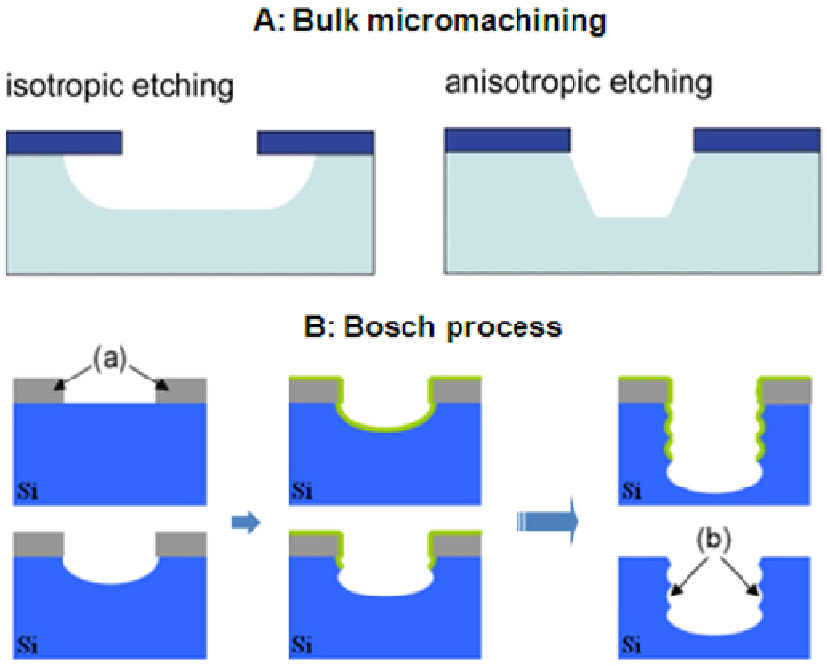


Figure 1.10: Illustration of bulk micromachining (A) and Bosch process (B).

Surface micromachining, on the other hand, comprises a number of techniques to build microstructures from thin films previously deposited on substrates (Figure 1.11). General process involves a sacrificial layer technique. Common sacrificial materials include silicon oxide, metal, and photoresist, which can be removed using chemicals. After a sacrificial layer is deposited and patterned on a substrate, structural thin film can be deposited and patterned, which will perform the mechanical or electrical function in the final device. Structural materials normally include silicon oxide, nitride, and polymer.

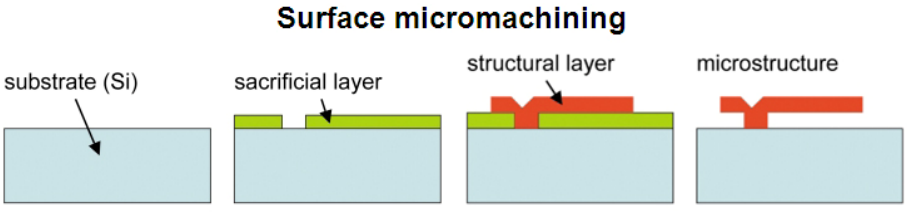
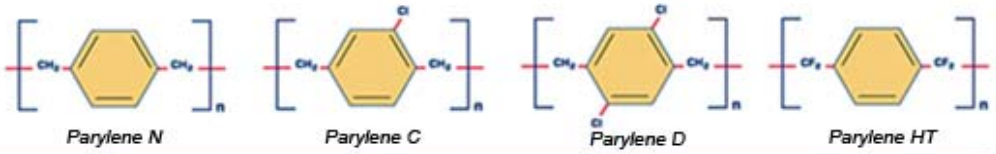


Figure 1.11: Illustration of surface micromachining.

Most devices described in this dissertation will use surface micromachining with Parylene C as the main structural material. Silicon only serves as a carrier, which will be completely removed after fabrication. System integration involves both surface and bulk micromachining technologies as the Bosch process would be used to etch through cavities for holding discrete components (capacitors, ASICs, etc.).

1.3.2 **Introduction to Parylene C**

Parylene is the trade name for a family of polyxylylene polymers, which were discovered in 1947 and commercialized by Union Carbide Corporation in 1965 [33]. To date, four types of Parylene dimer are commercially viable: Parylene N, Parylene C, Parylene D, and Parylene HT. The deposition takes place at room temperature using a chemical vapor deposition process, known as Gorham process. Raw material dimer is placed in a vaporizer furnace, and evaporated to a dimeric gas under vacuum. The gas then passes through a high temperature pyrolysis furnace, where the molecule is cleaved into monomers. The monomers enter a room temperature deposition chamber, and polymerize on all exposed surfaces inside the chamber conformally [34]. The un-reacted monomers are collected to a cold trap before they enter the mechanical pump. Parylene coating thickness normally ranges from one to tens of microns, controlled by the amount of the dimer. Deposition rate is proportional to the monomer concentration, correlated with the deposition chamber pressure. Different deposition parameters are required for various types of Parylene, but the process steps essentially remain the same (Figure 1.12).



	Parylene N	Parylene C	Parylene D	Parylene HT
Vaporizer	170°C	170°C	170°C	155°C
Pyrolysis	650°C	690°C	700°C	750°C

Figure 1.12: Chemical structures of Parylene N, C, D, and HT, and some of the correlated process parameters used in Parylene deposition system PDS 2010 and 2060.

Table 1.1: Properties of Parylene N, C, D, HT, and PDMS. (Table adopted from [35])

Property	Parylene-N	Parylene-C	Parylene-D	Parylene HT	PDMS
Dielectric Strength (V/mil), 1 mil film	7,000	5,600	5,500	5,400	610 (1 mm film)
Dielectric Constant					
60 Hz	2.65	3.15	2.84	2.21	
1 kHz	2.65	3.10	2.82	2.20	2.3-2.8
1 MHz	2.65	2.95	2.80	2.17	
Young's Modulus (psi)	350,000	400,000	380,000	--	52 – 126
Index of Refraction	1.661	1.639	1.669	--	1.4
Yield Strength (psi)	6,100	8,000	9,000	--	325
Elongation to Break (%)	20-250	200	10	--	210 – 310
Coefficient of Friction					
Static	0.25	0.29	0.33	0.145	--
Dynamic	0.25	0.29	0.31	0.130	0.43-0.51
Density (g/cm^3)	1.10-1.12	1.289	1.418	--	$9.7*10^{-4}$
Melting Point (°C)	420	290	380	>450	-49.9 – 40
Thermal Conductivity at 25 °C (10^{-4} cal/(cm*s*°C))	3.0	2.0	--	--	3.6
Water Absorption (% after 24 hours)	< 0.1	< 0.06	< 0.1	< 0.01	-- (depends on cure conditions)
Specific Heat at 20 °C (cal/g*°C)	0.20	0.17	--	--	0.35

The properties of different types of Parylene are summarized in Table 1.1, compared with poly(dimethylsiloxane)(PDMS). It can be seen that Parylene, and

specifically, Parylene C, has many desirable properties for neural prostheses compared with two other commonly used materials, PDMS and polyimide [36]. It has pinhole-free comformal deposition, low gas and water vapor permeability, and chemical inertness, so that it can protect implanted devices and electronics from interacting with body fluids or interfering agents. Its good mechanical strength (elongation break of 200%) and low Young's modulus (~4 GPa) make devices strong enough to survive surgical manipulations, and flexible enough to minimize damages to surrounding tissues. It is also optically transparent, allowing the anatomy to be seen though devices during implantation and follow-up. Most importantly, Parylene C is an ISO 10993 and United States Pharmacopeia (USP) Class VI biocompatible material, the highest biocompatibility and implant clearance among plastics. In fact, animal studies have been done to verify its biocompatibility in the eye environment. The experiments were conducted at Doheny Eye Institute of USC, by implanting untreated Parylene C thin films in the vitreous cavity of the right eyes of two rabbits. The thin films were left in the eyes for six months before the animal models were sacrificed. Post-mortem histological evaluation reveals no discernable difference between the retinas of experimental eyes and control eyes, indicating no detectable adverse immune response caused by implanted Parylene C (Figure 1.13). This result further strengthens the fact that Parylene C is biocompatible for intraocular retinal prostheses as well as other ocular implants.

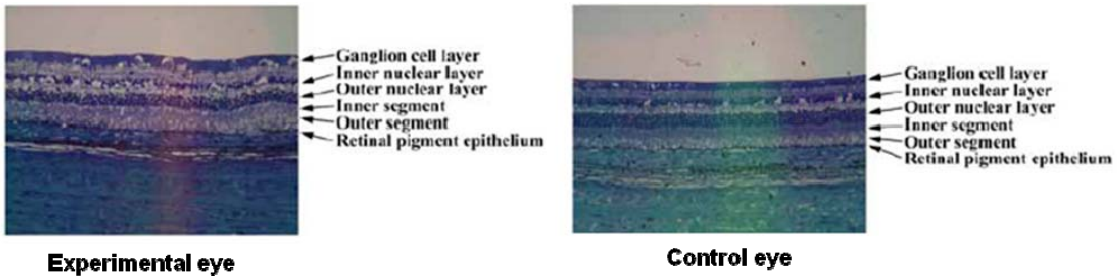


Figure 1.13: Typical morphology of rabbit retinas after six month implantation. (Images courtesy of Dr. Damien Rodger)

1.3.3 **Parylene-based MEMS for neural prostheses**

Parylene-C is originally used as an insulating and packaging material in the electronics industry. In recent years, there has been great interest in using Parylene-based MEMS for neural implant applications, where Parylene serves not only as a protecting layer, but also as a primary structural material.

The main advantage of using Parylene in MEMS fabrication lies in its ease of integration with other microfabrication techniques. The unique room-temperature conformal deposition characteristics make it post-COMS compatible, so that electrodes, sensors, actuators, and even circuit can be incorporated into Parylene devices. Furthermore, Parylene can be easily patterned with oxygen plasma etching, using either photoresist or metal as masks. However, one major concern is the adhesion between Parylene and other materials commonly used in MEMS fabrication. It has been found that the adhesion of photoresist and Parylene is generally good; whereas some materials, such as silicon oxide, evaporated gold and aluminum do not adhere to Parylene very well. To address the adhesion problem, several techniques and adhesion promoters have been developed. For instance, a saline-based adhesion promoter (A-174) can create good

bonding strength between Parylene and many substrates. Physical surface roughening using oxygen plasma, bromine trifluoride or Xenon difluoride can also help improve the dry adhesion between different layers of Parylene, as well as Parylene and silicon surfaces [37]. Consequently, devices with multi-layer Parylene structures can be implemented without special planarization techniques.

A large variety of devices have been built for neural prostheses using Parylene micromachining, such as electrodes for cochlear implantation [38], Parylene cabled neural probes [39] for cortical implantation, flexible multielectrode arrays for retinal and spinal cord implantation [35]. More Parylene-based devices and technologies will be discussed in this dissertation.

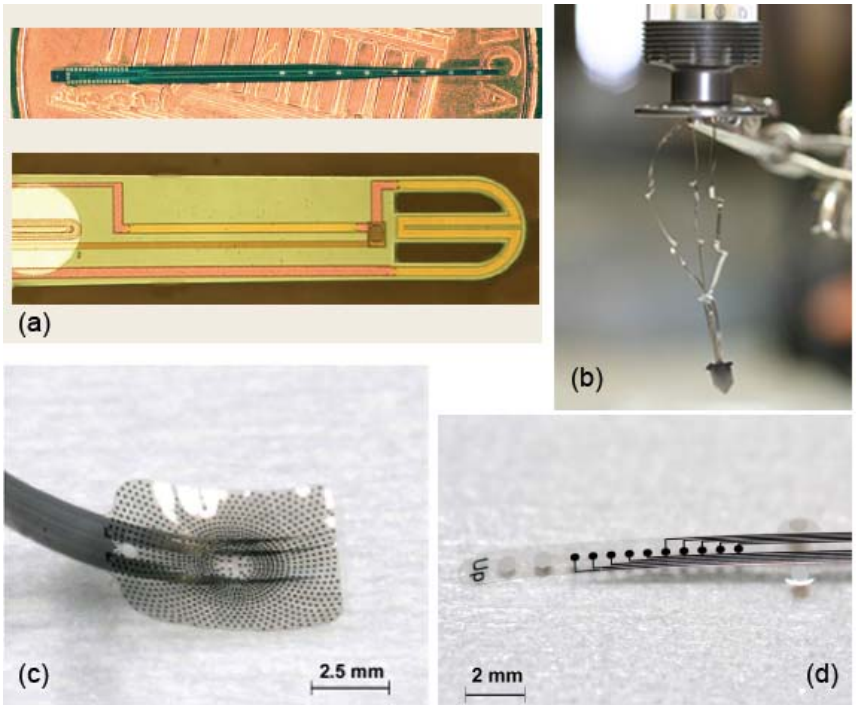


Figure 1.14: Parylene-based devices for neural prostheses: (a) cochlear probe; (b) 3-D neural probe; (c) retinal multielectrode array; (d) spinal cord electrodes.

1.4 Goal and layout of the dissertation

Our solution to the advanced retinal prostheses is to develop an all-intraocular system using Parylene-based MEMS technologies. The system, as shown in Figure 1.15, would comprise two MEMS radio-frequency (RF) coils for receiving wireless power and data signal, circuitry integrated on a flexible Parylene cable for converting the signal to simulation pulses, and a high-density MEMS electrode array for simulating the neural cells. The electrodes array has already been invented by Dr. Damien Rodger in the Caltech Micromachining laboratory [35]. Therefore, this work will center on MEMS Parylene-based technologies for RF coil fabrication and full system integration, which aim to contribute to the overall initiative of realizing neural prosthetic systems and particularly, an all-intraocular epiretinal implant system.

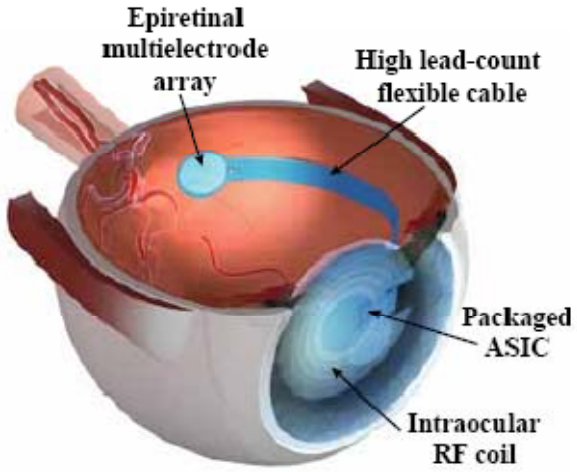


Figure 1.15: Proposed all-intraocular system for high density epiretinal implant. [35]

Chapter 2 describes the fabrication technology and the long-term reliability of a Parylene-metal-Parylene skin, which is a basic structure for planar Parylene MEMS device, such as electrode arrays and coils. Chapter 3 discusses the design procedure of the MEMS

coil from a theoretical point of view using analytical models, followed by Chapter 4, where coil prototypes are experimentally designed, fabricated and measured. Chapter 5 introduces a wafer level integration technology, enabling the integration of application-specific integrated circuits (ASICs) with other system components. We also present the detailed design, fabrication and functional testing of a full implantable, flexible, Parylene-enabled neurostimulator that features single channel wireless stimulation capability in Chapter 5.

1.5 Summary

Two blindness diseases due to outer retinal degeneration are described in this chapter. Research shows that the visual prosthesis technology has great potential for treating these diseases and restoring the lost vision function. Four visual implantation approaches are discussed, among which the epiretinal retinal prosthesis has distinct advantages over others. However, a number of obstacles still exist, mainly related to material choice and fabrication development. Therefore, an all-intraocular epiretinal implant system is proposed to address these issues, utilizing Parylene-based MEMS technologies for device fabrication and system integration.

Chapter 2 PARYLENE-METAL-PARYLENE SKIN AND ITS LONG-TERM BIOSTABILITY

2.1 Introduction

As discussed in Chapter 1, one of the main goals of this work is to develop MEMS RF coils as receiver coils for wireless power and data transfer. A key technology for making such coils is so called a flexible Parylene-metal skin technology, featuring a Parylene-metal-Parylene sandwich structure. In this chapter, we will present the detailed process for making Parylene-metal-Parylene skins. The feasibility of using these skins for long-term implantation is also studied using an accelerated lifetime soaking test (ALST).

2.2 Parylene-metal-Parylene skin technology

2.2.1 Review of flexible MEMS skin technologies

The flexible MEMS skin technology refers to a microfabrication technology that enables the integration of MEMS devices and ICs onto a flexible skin normally made of polymer materials. The concept was first proposed in 1985 by Barth et al., in which a one-dimensional flexible Si-diode temperature sensor array was built using a polyimide strip to connect Si islands formed by isotropic HNA etching [40]. However, their technology has serious reliability problems and needs major improvements. In 1997, Jiang et al. reported the results of a remarkable work, where a reliable, large scale 2-D shear stress sensor skin was developed and successfully demonstrated for use in aerodynamic applications [41]. As a follow up of this study, an IC-integrated shear-stress sensor skin was invented, showing the capability of integrating CMOS circuitry on the flexible skin [42].

The fabrication process, as illustrated in Figure 2.1, uses polyimide as structural layers, connecting Si islands formed by selective wet etching (KOH or TMAH) or plasma dry etching (DRIE) [43]. Planar MEMS structures, such as electrode contacts and metal leads, will be directly fabricated on the polymer substrate. Si MEMS devices, such as ICs, Si sensors and actuators, will be processed on the Si islands.

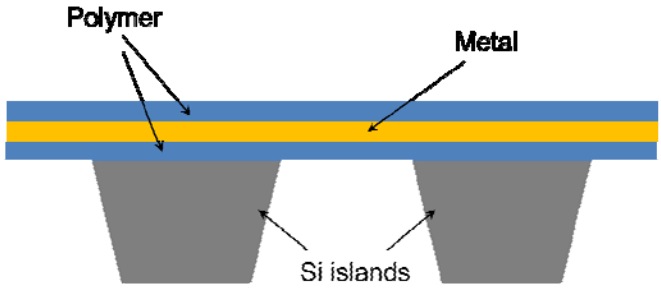


Figure 2.1: Illustration of the flexible MEMS skin technology.

A big advantage of this process is that it is compatible with other MEMS technologies so that only minimal adjustments are needed in order to build flexible MEMS skins. However, this process is not applicable to retinal implants because the biocompatibility of silicon is arguable although some evidences have shown that bare silicon can support cell growth [44]. Recent efforts on flexible MEMS skins use polyimide as substrate and completely remove the silicon substrate [45, 46], but they still need to tackle the long-term biocompatible difficulty of the polyimide. Therefore, it is necessary to develop a fully implantable MEMS skin technology and Parylene emerges as a good candidate because of its many desirable properties.

2.2.2 **Process development**

Parylene-metal-Parylene skins will typically involve thin-film metal structures sandwiched by Parylene C, as shown in Figure 2.2. For simplicity, only one layer of metal is drawn to illustrate the concept. For actual devices in general, multiple layers can be achieved, which will be further discussed in Chapter 4.

Figure 2.2: Conceptual illustration of Parylene-metal-Parylene skins.

A typical fabrication process for making such skins with one layer of metal is depicted in Figure 2.3. First, a layer of AZ4400 photoresist (AZ Electronic Materials, Branchburg, NJ, USA) is optionally spun on a standard silicon wafer as the sacrificial layer, and hard baked at 100ºC for overnight. After that, a layer of Parylene C is vapor-deposited in a PDS 2010 system (Specialty Coating Systems, Indianapolis, IN, USA) on top of the photoresist, followed by metal deposition using an e-beam evaporator (SE600 RAP, CHA Industries, Fremont, CA, USA). An AZ 1518 layer is then spun on top of the metal, exposed in a 10× reduction GCA Mann 4800 DSW wafer stepper (General Signal Corporation, Stamford, CT, USA), or a Kasper 2001 contact aligner (Kasper Instruments, Inc., Sunnyvale, CA, USA), depending on the resolution requirement of metal features, and developed to form a photoresist mask for metal etching. After metal patterning, the

photoresist mask is removed, and another layer of Parylene C is deposited to seal the entire metal structure. A photoresist etch mask is then spun and patterned to expose the areas of the contact pads, as well as to define the device profile. Finally, unwanted Parylene is etched using oxygen plasma in a reactive ion etch (RIE) system (Semi Group Inc. T1000TP/CC), and the entire flexible structure is released from the silicon substrate by dissolving the photoresist sacrificial layer using a standard acetone etch process. If no sacrificial photoresist is applied, devices can be directly peeled from the natively oxidized silicon substrate in a water bath due to the hydrophobicity of the underlying Parylene C surface.

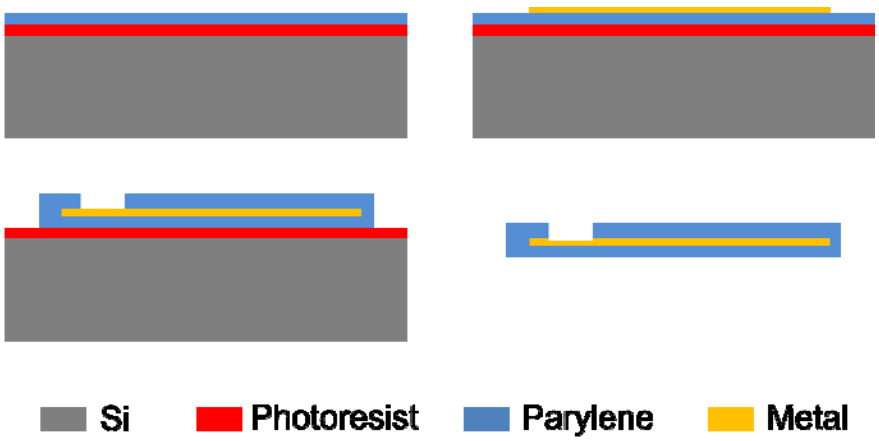


Figure 2.3: Fabrication process of Parylene-metal-Parylene skin technology.

The Parylene-metal-Parylene skin technology serves an important role in the Caltech Micromachining Laboratory, and many devices have been developed using this technology, such as multielectrode array skins and flexible Parylene cables. For the retinal prosthesis project, this technology has its distinct advantages. First, by using Parylene directly as the actual substrate, both the fabrication and packaging procedures of the device can be greatly simplified. Additionally, the skins are flexible and foldable so that they can

be implanted through small surgical incisions, allowing wounds to heal quickly. Moreover, the metal lines are completely padded by the flexible Parylene material, and can therefore with stand repeated bending during surgical handling. Finally, a heat-molding treatment, which will be discussed in Section 2.3.3 , has been developed to modify the skins into various shapes, allowing them to easily match the curvature of the target implant area.

2.2.3 **Adhesion issue on interfaces**

With the Parylene technology at hand, the next step is obviously to investigate its long-term reliability because human body, fairly well approximated by an oxygenated saline solution with a salt content of about 0.9% at pH ~ 7.4 and temperature of 37±1 ºC [47], is a harsh environment for metals. Although researches have been done to evaluate the biostability of Parylene packaging in the past years [48, 49], the long-term reliability of such Parylene-metal-Parylene sandwich structures has never been studied.

Initial experiments to test the Parylene sealing behavior are carried out by soaking Parylene bi-layer samples in hot saline, which is a close imitator of body fluids. Serious delamination and water bubbles are found at the Parylene-Parylene interface (Figure 2.4(a)) of samples without any treatment, indicating that the Parylene sealing is not hermetic. It is also found, however, if the bi-layer films are treated with an annealing process for 3 days at 200 ºC in a vacuum oven (T-M Vacuum Products, Inc., Cinnaminson, NJ, USA), no interfacial delamination or water bubbles can be detected even after months of soaking (Figure 2.4(b)). This preliminary evidence reveals that high temperature annealing might be one of the approaches to improve Parylene sealing quality. In order to fully understand Parylene packaging behavior in saline, as well as to optimize the process for improving

Parylene sealing behavior, many experiments have been done which will be described in the following sections.

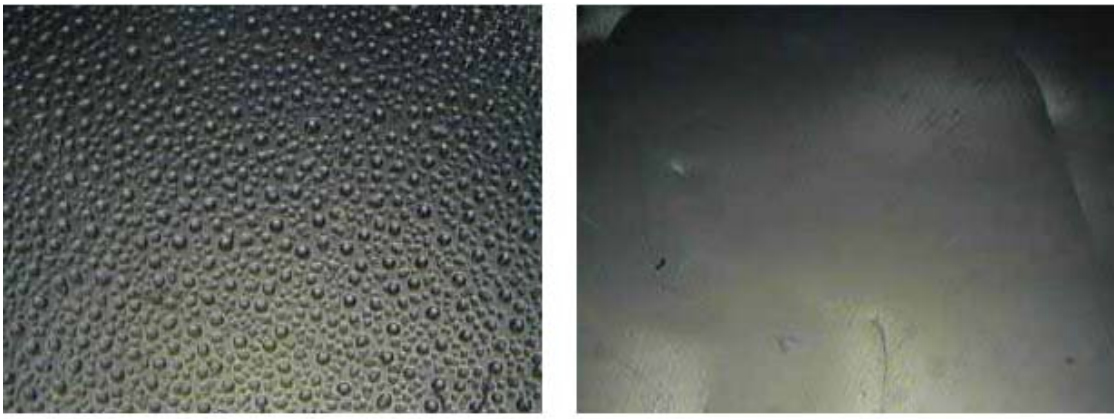


Figure 2.4: (a) Untreated Parylene bi-layer sample after one day soaking. Water bubbles are formed at the interface. (b) Annealed Parylene-bi-layer sample after long-term soaking. No delamination or water bubble is observed.

2.3 Interfacial adhesion enhanced process

2.3.1 Accelerated-lifetime soaking test of Parylene bi-layer structures

A matrix of Parylene-bi-layer samples is designed and investigated under accelerated lifetime conditions to find reasonable process conditions for interfacial adhesion improvement. The samples are simply prepared by coating ~6 μm Parylene C on standard silicon wafers, followed by various processes on the Parylene surfaces. After that, another ~6 μm of Parylene C is deposited on top. Then bi-layer films are peeled from the wafers and cut into strips for test. Table 4.1 summarizes the preparation procedures of different samples, where oxygen plasma roughening is done in a PEII-A plasma etcher (Plasma Equipment Technical Services Inc., Livermore, CA, USA). This roughening process serves the purpose of increasing mechanical adhesion between the two Parylene

layers. In addition, ultrasonic and/or buffered HF cleaning are performed on some samples to remove contaminants and organic residues. Before testing, the samples are selectively annealed in the vacuum oven at setting temperatures ranging from 80 ºC to 260 ºC with different heating durations. The total chamber pressure is controlled to be approximately 10 Torr with nitrogen backfill, which is sufficient to prevent oxidative degradation of Parylene C at high temperatures (>120 ºC) in air.

Table 2.1: Samples preparation of Parylene bi-layers for soaking tests.

Sample set	Parylene deposition	Treatments			Parylene deposition
		O2 plasma 200 mTorr, 400 W	Ultrasonic in water bath	Buffer HF dip	
1	6 μm	N/A	N/A	N/A	6 μm
2	6 μm	2 min	N/A	N/A	6 μm
3	6 μm	N/A	5 min	N/A	6 μm
4	6 μm	N/A	N/A	20 sec	6 μm
5	6 μm	2 min	5 min	N/A	6 μm
6	6 μm	2 min	N/A	20 sec	6 μm
7	6 μm	2 min	5 min	20 sec	6 μm

The tested samples are held in centrifuge tubes filled with regular saline, and measurements are conducted in a convection oven at 77 ºC, as shown in Figure 2.5. During first month of soaking, the samples are removed daily from the saline for inspection using optical microscopy, and then at one-week intervals for the rest of soaking lifetime. To maintain a constant NaCl concentration, the test cells are cleaned and replenished once a

week. These tests have been continued for up to two years, and sample lifetimes are recorded when delamination or water bubbles are seen at the interfaces. Five samples are tested in each set, and their mean-time-to-failure (MTTF) is summarized in Table 2.2.

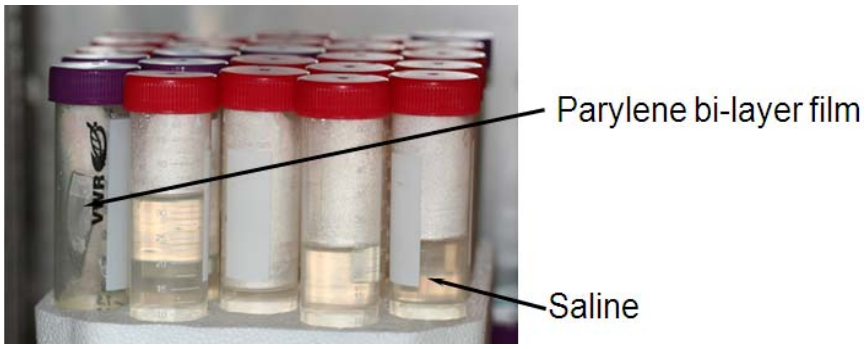


Figure 2.5: Testing cells of Parylene bi-layer samples are placed in a convection oven.

Table 2.2: Accelerated-lifetime soaking test results of Parylene bi-layer samples. Red color denotes failed samples. Blue color denotes good samples.

Sample set	Annealing Treatments										
	80 ºC		140 ºC		180 ºC		200 ºC		260 ºC		
	12 hours	2 days	12 hours	2 days	12 hours	2 days	12 hours	2 days	1 hour	12 hours	2 days
1	2 Y*	2 Y	2 Y	2 Y	2 Y	2 Y	2 Y	2 Y	2 Y	2 Y	2 Y
2	1 D**	1 D	1 D	2 D	1 D	1D	1 D	1 D	1 D	5 D	2 Y
3	2 Y	2 Y	2 Y	2 Y	2 Y	2 Y	2 Y	2 Y	2 Y	2 Y	2 Y
4	2 Y	2 Y	2 Y	2 Y	2 Y	2 Y	2 Y	2 Y	2 Y	2 Y	2 Y
5	1 D	1 D	1 D	1 D	2 D	2 D	5 D	7 D	14 D	80 D	2 Y
6	1 D	1 D	1 D	2 D	7 D	40 D	21D	2 Y	2 Y	2 Y	2 Y
7	1 D	1 D	1 D	6 D	21 D	2 Y	2 Y	2 Y	2 Y	2 Y	2 Y

*: Year

**: Day

From the test results, we find that O_2 plasma roughening tends to exaggerate the delamination problem probably due to particle contaminants. Annealing at temperatures higher than 180 ºC can significantly improve chemical adhesion between Parylene and Parylene, even when devastating processes, such as O_2 plasma roughening, are performed. As the temperature goes up, the process can convert poor-behaving samples into well-behaving ones within a short time. It is of note that the annealing temperature has to be lower than the melting temperature of Parylene C (290 ºC), as strong recrystallization of Parylene C can happen beyond this point [50, 51], resulting in brittle Parylene C. Besides annealing, interface cleanness is also an important factor in order to ensure a good adhesion between two Parylene layers.

According to the results of this test matrix, a routine procedure for optimizing Parylene adhesion is determined as follows:

1) Before subsequent Parylene deposition, buffered or diluted HF (10%) cleaning is necessary if microfabrications, such as O_2 plasma roughening, photoresist processing, or chemical treatments, have been done at Parylene interface.

2) Post-fabrication annealing treatment needs to be performed in a vacuum oven for 2 days at 200 ºC.

Mechanisms by which annealing treatment can improve Parylene to Parylene adhesion are still not completely understood. However, there are several hypotheses to explain it. First, as can be seen from the results, annealing process takes effect at temperatures beyond the glass-transition temperature of Parylene C (80-100 ºC) [52]. As a result, material reflowing could be accelerated at the interface, and polymer interweaving

between two Parylene layers could be increased. It is also possible that this process could provide sufficient thermal energy for activated ends of polymer strands at the interface to bond with each other. Finally, this annealing process might bake unpyrolyzed Parylene dimer out of the interfacial regions. All these effects, essentially, serve the purpose to convert the non-homogeneous two-layer structures into a more homogeneous bulk-like material. Consequently, water trapping at the interface could be reduced as most of water would pass through it instead [35]. However, it is hard to experimentally verify these hypotheses due to a lack of effective techniques to analyze interface properties.

It is also well known that polymers tend to increase their density when heated and then re-cooled, especially if the excursion is beyond the glass transition temperature of the material. This fact suggests that the high temperature annealing might make Parylene denser so that water cannot permeate through thin films. An experimental setup is designed based on the water cup method to verify this hypothesis, and the experimental details and some of the preliminary results will be discussed in the next section.

2.3.2 **Water vapor permeation through thin-film Parylene C**

Water vapor permeability is one of the important aspects to evaluate Parylene barrier properties, and particularly, water vapor transmission rate (WVTR) has been widely used as a measure for water vapor permeation of Parylene in the past. Table 4.1 gives reported WVTR values for Parylene C from literatures. However, all these data, which are measured from fresh Parylene C materials, are not applicable to annealed Parylene C. In addition, the water vapor permeability (WVP) of a polymer thin film depends greatly on

deposition quality and post-process conditions. Hence, studies need to be done in order to understand the permeability properties of our Parylene C.

Table 2.3: Published WVTR data for Parylene C. (Courtesy of Parvathy Menon).

Parylene C WVTR (g-mil/100in2-day)	WVTR at 37 ºC, 90%RH	Year of publication	Measured/company stated
Hubbell et al. [53]	3.3-7.3	1975	Measured
Loeb et al. [54]	0.5	1977	Company (Union Carbide)
SCS [35]	0.21	2004	Company
SCS [55]	0.203	2007	Company
Caltech [56]	0.207	2008	Company (Illinois Instruments)

A simplified water cup experiment has been designed to test Parylene WVTR in house. The experiment is performed in a small beaker filled with approximately 40 mL of DI water. The beaker opening is covered with a piece of Parylene C thin film and sealed with 5-minute dry epoxy. During the measurement, the beaker is stored in the cleanroom environment to maintain a constant relative humidity of 30% and a temperature of 20 ºC, and is weighed at distinct intervals using a Mettler analytic balance (Mettler Instrument Corp., Hightstown, NJ) to obtain its weight loss. Then WVTR is calculated and normalized to film thickness using the following equation [57].

$$WVTR = \frac{MassLost}{Time \times Area} \times Thickness \qquad 2\text{-}1$$

Table 2.4: Average WVTR of Parylene C thin films prepared under different conditions. Each sample set contains 2 samples from a same batch of Parylene deposition. (Data courtesy of Menon Parvathy[56].)

Tested sample set	Annealing treatment	Avg. WVTR (g-mil/100in^2-day)	WVTR reduction
9 μm Parylene C	N/A	0.0638	
9 μm Parylene C	200 ºC for 2 days	0.0387	39.4%
18 μm Parylene C	N/A	0.0695	
18 μm Parylene C,	200 ºC for 2 days	0.0435	37.4%
18 μm bi-layer Parylene C	200 ºC for 2 days	0.1032	

Various types and preparations of Parylene C are tested, and preliminary results are listed in Table 2.4. The results confirm that the annealing treatment indeed reduces the WVTR of Parylene C, and therefore improves Parylene water barrier properties by reducing perpendicular permeation through the thin films. A 9 μm film shows a WVTR reduction of ~40%, and similarly, an 18 μm Parylene sample shows a ~37% reduction. Comparing the bi-layer samples with the single layer samples, it is also found that the average WVTR of the bi-layer samples is approximately 60% higher, indicating Parylene to Parylene interface is not perfectly homogeneous even after annealing.

This is the first experiment in which we are able to measure the WVTR of annealed Parylene, and the preliminary results show consistency with the soaking test results. Because WVTR is a function of system partial pressure and temperature, with a given WVTR under one condition, it is impossible to predict permeability properties under different conditions. Further measurements at various temperatures are underway. With

more data, we should be able to determine the activation energy of permeation, and moreover, to extrapolate WVTR reasonably well.

2.3.3 **Parylene heat molding**

Another application of annealing treatment is Parylene heat molding. For biomedical applications, particularly, for intraocular implantations, Parylene devices, such as coil, electrode arrays and Parylene cables, needs to be modified into a curvature similar to that of the eye in order to meet surgical and comfort requirements. Instead of using prohibitively-difficult 3-D fabrication, Parylene C can be directly contoured and confined with an existing metal mold to achieve desired geometries. This heat molding technology will facilitate the device design and surgical procedures for human implantation, because different curvatures can be easily achieved by varying the size of molds to match the actual dimension of patients' eyes.

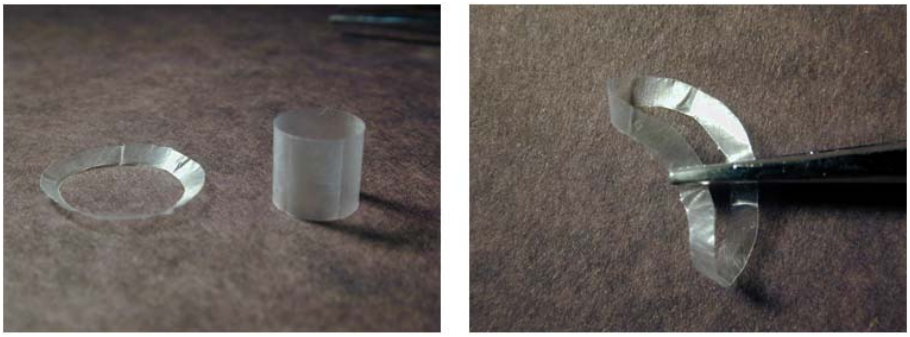


Figure 2.6: Examples of Parylene heat molding: (*left*) Different shapes are formed for Parylene films. (*right*) Demonstration of flexibility after heat molding.

Figure 2.6 (a) shows Parylene C films after heat molding at 200 ºC for 2 days. With the aid of metal molds, Parylene films can be formed into spherical or cylindrical shapes. In fact, it has been proven that this conformation is permanent due to Parylene glass transition, and therefore the conformation can be maintained throughout sterilization,

implantation, and follow up examination [35]. Additionally, as can be seem from Figure 2.6 (b), Parylene C still remains flexible after heat molding. We have also done heat molding for actual Parylene-based devices, as presented in Chapter 5.

2.4 Accelerated-lifetime soaking test of Parylene-metal-Parylen skins

2.4.1 Sample preparation

Although we have demonstrated that the annealing process can significantly enhance Parylene to Parylene adhesion, no evidence shows that this process can be used to improve Parylene packaging behavior for embedded metals. As Parylene-based components in the retinal implant, such as RF coils and electrode arrays, normally involve Parylene-metal-Parylene sandwich structures, this is a crucial void in knowledge that must be addressed.

To study the biostability of Parylene-protected metal, ALSTs have been done using a thin film resistor structure, which employs metal traces encapsulated by Parylene C. Samples are microfabricated in the same manner as described in Section 2.2.2 (Figure 2.7). Various samples are prepared with different metal combinations, Parylene thicknesses and post-fabrication treatments, as summarized in Table 2.5.

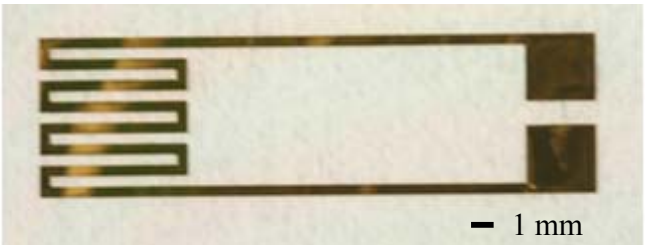


Figure 2.7: A Parylene packaged thin film resistor with pure gold metallization.

Table 2.5: Sample preparations.

Sample set	Metallization	Parylen thickness (μm)	Annealing treatment
1	Ti-Au-Ti	~ 4.7	N/A
2	Cr-Au-Cr	~ 4.7	N/A
3	Pure Au	~ 4.7	N/A
4	Ti-Au-Ti	~ 4.7	2 days, 200 ºC
5	Cr-Au-Cr	~ 4.7	2 days, 200 ºC
6	Pure Au	~ 4.7	2 days, 200 ºC
7	Ti-Au-Ti	~ 9.2	2 days, 200 ºC
8	Cr-Au-Cr	~ 9.2	2 days, 200 ºC
9	Pure Au	~ 9.2	2 days, 200 ºC

2.4.2 **Passive soaking test of Parylene-protected metal**

Samples are first tested passively in saline at temperatures of 77 ºC and 90 ºC respectively. To monitor their failures, the devices are removed from ovens daily, and observed optically under a microscope. Failure mechanisms of various samples are shown in Figure 2.8. Bubbles and delamination are first seen when failure is initiated in tested samples, mainly due to moisture permeation through Parylene C films or the Parylene-Parylene interface. After that, metal corrosion is continuously propagated in the samples that contain adhesion promotion layers, namely titanium or chromium. The mechanisms of metal corrosion in body fluids have been studied by Mudali et al., and the results suggest that the corrosion is mainly caused by metal ionizations due to redox reactions or metal chloride breakdown [47]. Typical reduction potentials of Ti and Cr have been reported to be -1.630 V (Ti^{2+}) and -0.913 V (Cr^{2+}) respectively, which are much lower than that of Au

(1.498 V for Au^{3+}) [58]. Therefore, Ti and Cr are easier to get oxidized when exposed to saline, which is consistent with our measurement results.

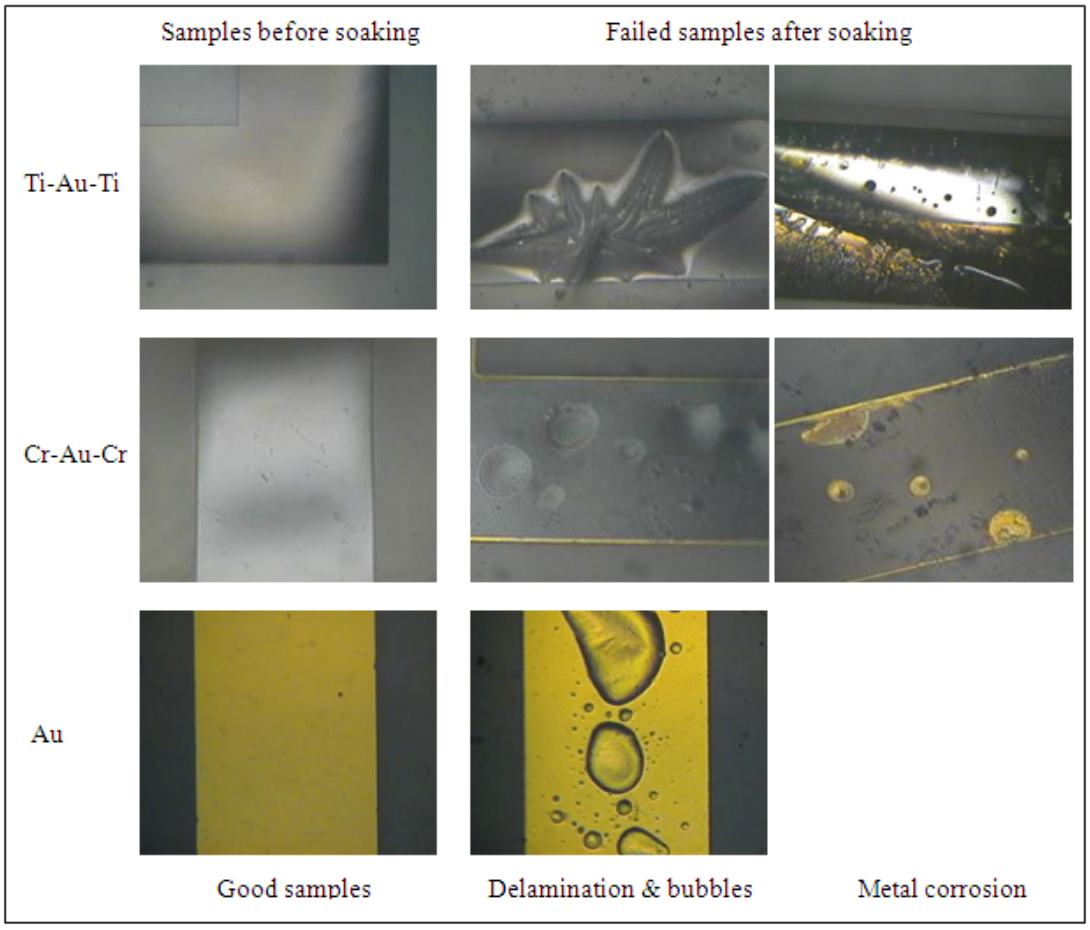


Figure 2.8: Microscope images of samples before and after passive ALSTs, showing different corrosion mechanisms.

In each sample set, 5 samples are measured and their MTTF is recorded when the failure are seen (Table 2.6). With known MTTF at two temperature points, an Arrhenius relationship can be used to extrapolate the MTTF at body temperature [59]. In this model, the MTTF at a given system temperature T (in Kelvin) can be expressed by equation 2-2, where A is the pre-exponential constant, E_a is the activation energy of failures (in eV),

and k is the Boltzman's constant (8.62×10^{-5} eV-K^{-1}). The activation energy of each sample set is calculated using the Arrhenius relations, and their MTTF at body temperature is predicted, as summarized in Table 2.6.

$$MTTF = A\exp(-\frac{E_a}{kT}) \qquad 2\text{-}2$$

Table 2.6: Soaking test results for Parylene-metal-Parylene structures under passive conditions, and extrapolated data according to the Arrhenius relationship.

Sample set	Average MTTF in saline		Calculated activation energy E_a(eV)	Extrapolated MTTF at 37 ºC
	77 ºC±2 ºC	90 ºC±2 ºC		
1	90 minutes	35 minutes	-0.80	~ 45 hours
2	3 hours	80 minutes	-0.68	~ 55 hours
3	69 hours	44 hours	-0.38	~ 14 days
4	80 days	23 days	-1.05	~ 20 years
5	>250 days	28 days	---	---
6	>250 days	70 days	---	---
7	>250 days	>250 days	---	---
8	>250 days	>250 days	---	---
9	>250 days	>250 days	---	---

The results show that the annealed samples from sets #5 and #6 have MTTF's at body temperature well over 20 years, indicating the annealing treatment can significantly enhance the Parylene packaging performance by improving moisture barrier behaviors at Parylene-metal interface as well as at Parylene-Parylene interface. For the samples coated with 9.2 μm Parylene C, no major physical damage or water bubbles are discovered even after 250 days of soaking, confirming that thicker Parylene films will have better moisture

barrier performance than thinner ones. Comparing the samples with various metal combinations, we have found that Parylene-protected gold has the activation energy of approximately -0.38 eV (36.66 kJ/mol). This value agrees with the activation energy of water vapor permeation through bulk Parylene C [56, 60], indicating the failure is most likely caused by the moisture permeation in this case. However, the samples with adhesion promotion metal show lower activation energies due to metal oxygen reduction, which has free energies of activation normally ranging from -0.68 eV (66 kJ/mol) to -0.83 eV (80 kJ/mol) for many metals [61, 62].

2.4.3 **Active soaking test of Parylene-protected metal**

Active soaking tests are also performed using a simplified electrochemical setup (Figure 2.9), in which one electrode is the Parylene thin film resistor, while a platinum wire severs as a reference electrode. To connect a sample to test equipments, conductive wires are glued onto contact vias with conductive epoxy, and sealed with insulating epoxy to prevent unwanted current leakage. A square wave with a magnitude of 6 Volts and a frequency of 50 Hz is continuously applied to form a potential drop across two electrodes. The test cell is heated in a convection oven at 90 ºC, and the sample's DC resistance is measured and recorded every 10 minutes using an HP 4145 B semiconductor parameter analyzer (HP/Agilent Technologies Inc., Santa Clara, CA) controlled by a LabView program (National Instruments, Austin, Texas). As we mentioned earlier, gold is the most favorable material for biomedical applications. Hereby, only sample sets with pure gold metallization (sample sets #3, #6 and #9) are tested under the active condition.

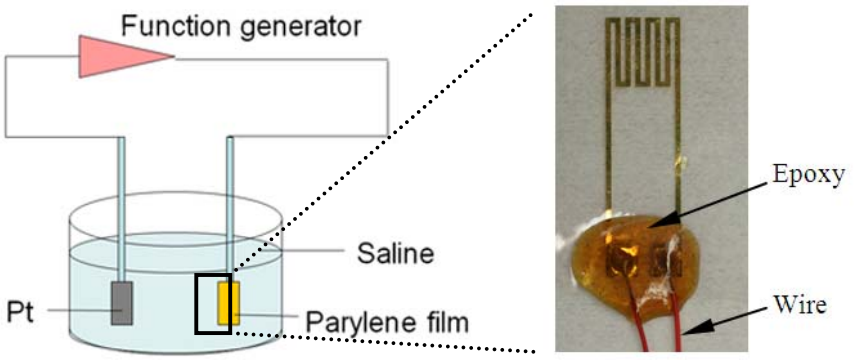


Figure 2.9: Simplified electrochemical test setup for active soaking test. A tested device is shown in the right picture.

Figure 2.10 shows a representative curve of temporal DC resistance changes for samples from three sets. The sample failure is defined as time points when resistance is within 30% from the original value before, and increases significantly after, usually by over 3 orders of magnitude. Again, the annealed sample with thicker Parylene sealing shows a much longer life-time compared with others, which is consistent with the result from passive tests.

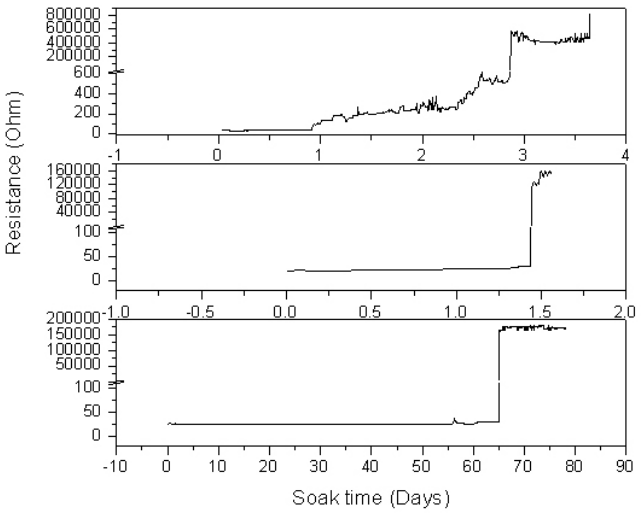


Figure 2.10: Typical aging curve of a sample: (*top*) from sample set #3. (*middle*) from sample set #6. (*bottom*) from sample set #9.

The failure mechanisms of samples under active soaking conditions are investigated using SEM and optical methods. Different failure modes are discovered in samples with different thicknesses of Parylene coating. The typical failure procedure on the samples with 4.7 μm Parylene is recorded at distinct day intervals using a Canon Digital Rebel XT camera (Canon Inc., Tokyo, Japan), as shown in Figure 2.11. Parylene breakdown is first seen after a short period of soaking, followed by Parylene delamination starting from the breakdown areas. Then metals are directly exposed to the saline and corrosion is observed. Finally, two Parylene layers are completely separated, and metal delaminates from Parylene.

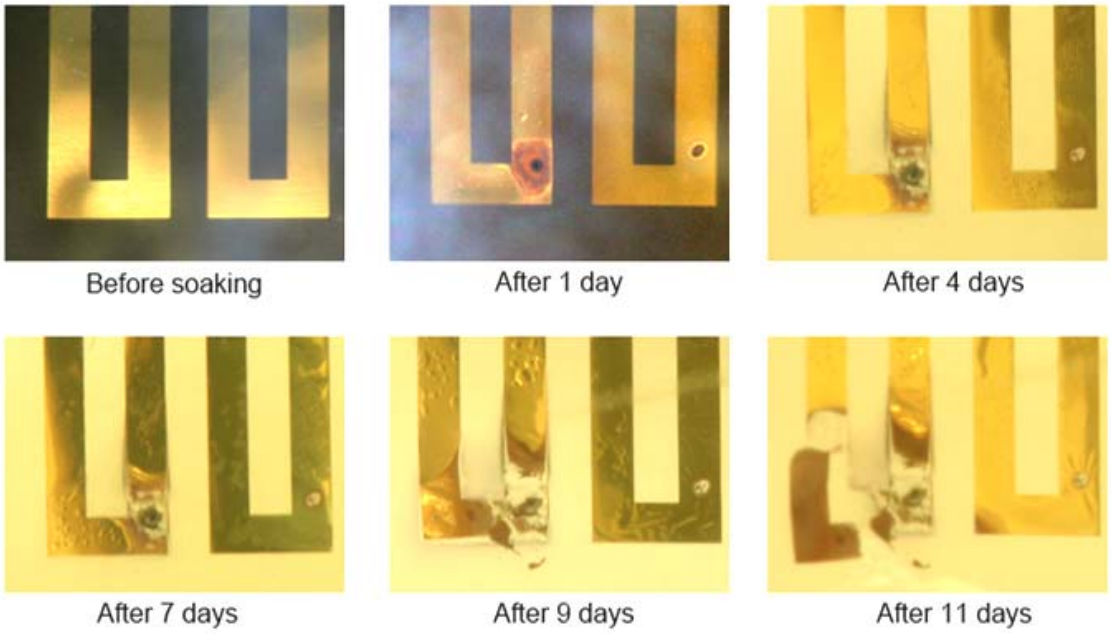


Figure 2.11: Failure procedure observed in sample with 4.7 μm Parylene coating.

The breakdown regions are also examined using scanning electron microscopy (SEM) and analyzed with energy dispersive X-ray spectroscopy (EDS), as shown in Figure 2.12. The EDS spectra confirm that the Parylene film is melted into a circular though-hole,

and the embedded metal is directly exposed. Parylene cracks radiate from the breakdown hole, which is probably caused by the thermal stress due to local heating. It should be noted that the breakdown hole is only observed on one side of the sample, while the other side remains intact, indicating the failure happens either on the interface or inside the Parylene film.

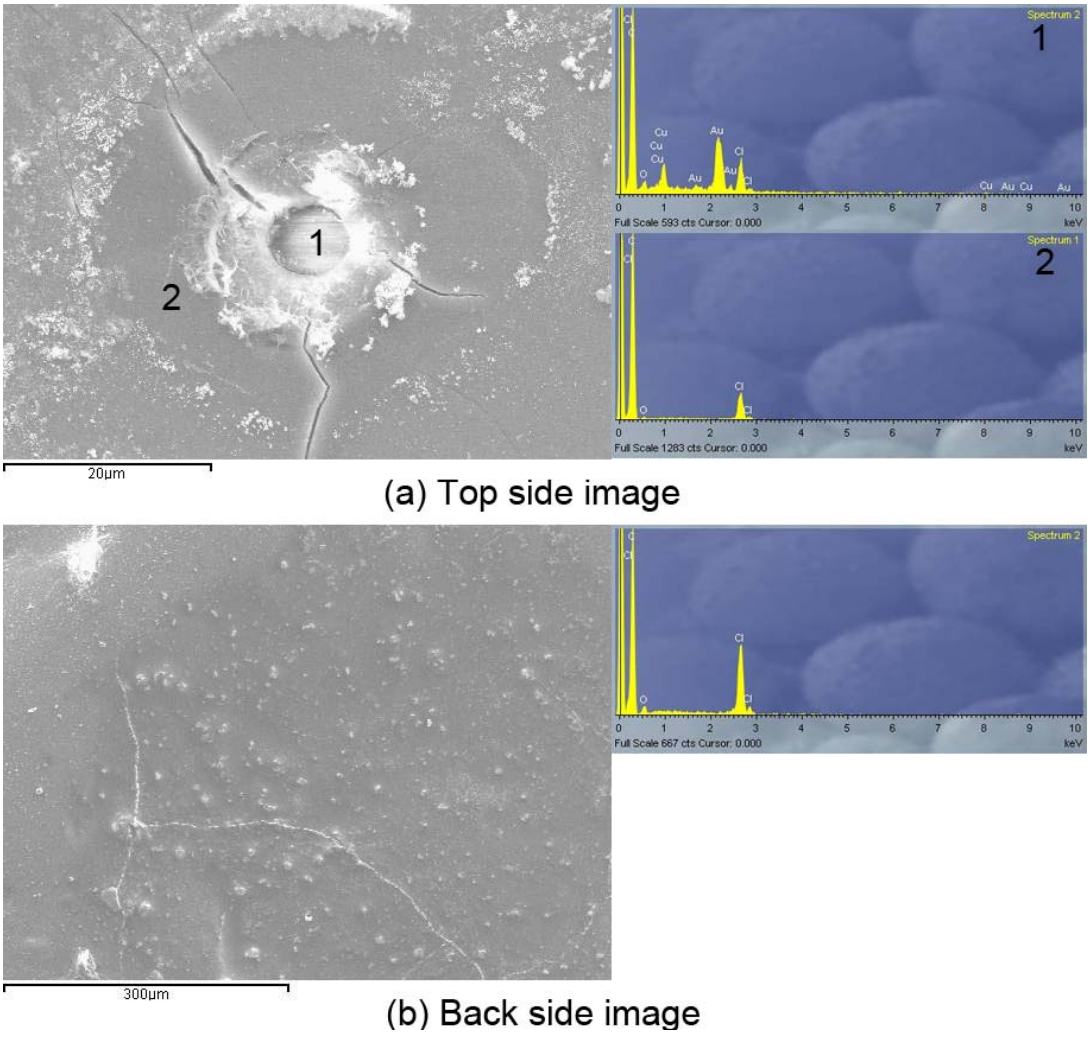


Figure 2.12: Typical SEM images and EDS spectra on the top side and the back side of the breakdown area.

Although the mechanism of the Parylene breakdown is not completely clear, we believe that it is defect-initiated breakdown because the breakdown is randomly located and localized in certain area where large defects and particles probably reside. Electrochemical reactions are accelerated at such points due to high electric field concentration and the direct exposure of metals to the saline, creating local metal corrosion. The breakdown hole has a diameter of over 6 μm (Figure 2.12 (a)), which implies that 4.7 μm of Parylene is not thick enough to cover some big defects or particles. Both annealed and unannealed samples show similar failure modes, indicating that the annealing process cannot help reduce defects or contaminant particles.

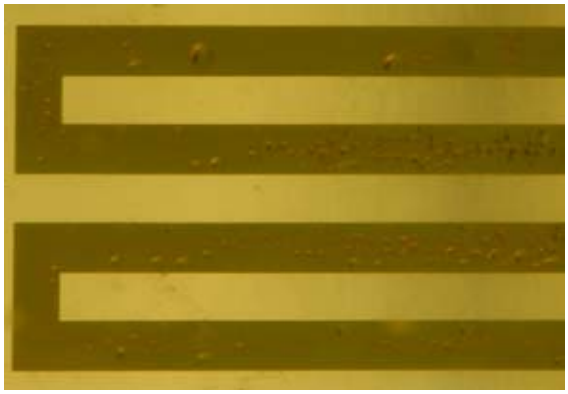


Figure 2.13: Even bubbles observed on samples from set #9 after soaking in saline at 90 ºC for 65 days.

As for samples with 9.2 μm Parylene coating, only water bubbles are observed uniformly across the whole metal-Parylene interface (Figure 2.13), which suggests that moisture diffusion becomes the dominant failure mechanism instead of Parylene breakdown. It is possible that dimensions of defects or particles are relatively small under cleanroom conditions so that thicker Parylene could conformally cover them. If we use the

activation energy of water vapor permeation that we derived from passive conditions before, samples in set #9 will have an MTTF at 37 ºC of approximately 62 years.

2.5 Summary

This chapter presented a Parylene-metal-Parylene skin technology, which is a key technology for making RF coils and multielectrode arrays in the retinal implant system. A standard procedure is also developed to improve the adhesion on Parylene-Parylene interface. To evaluate the long-term reliability of such Parylene-metal-Parylene skins, ALSTs are conducted in hot saline under various conditions. The results show that gold is less corrosive compared with titanium or chromium, and therefore is an ideal metal for biomedical applications. It is also found that annealing at 200 ºC for 2 days can significantly improve Parylene sealing behavior. In addition, Parylene film thicker than 10 μm is sufficient to cover small defects and particles produced from fabrication, preventing electrical breakdown in the devices. The MTTF's extrapolated using the Arrhenius model show that Parylene-protected gold can remain intact at body temperature for over 60 years, which is very encouraging for retinal implantation.

However, there are still outstanding issues that deserve closer investigations. First, the ovens used for testing have temperature variation of +/- 2 °C. Due to the exponential nature of the Arrhenius model, this temperature change can affect the prediction significantly. Precise temperature control is needed to achieve a more accurate prediction. Also, because this soaking test is time consuming, we only analyzed data from a small sample set for initial investigation. Long term continuous tests are necessary to collect more data, which will further refine our knowledge on Parylene packaging behaviors.

Chapter 3 DESIGN OF PARYLENE-BASED MEMS COILS

3.1 Introduction

In Chapter 2, we have developed the basic technology for making flexible MEMS coils, involving a Parylene-metal-Parylene sandwich structure. We also know that metal lines can be protected by Parylene C from corrosive environments. However, there are other constraints on the MEMS coil design such as physical size and coupling efficiency, which are by no means straightforward to achieve. In general, MEMS coils suffer from low inductance and noticeable parasitic effect, namely parasitic resistance and capacitance, due to the characteristics of planar MEMS fabrication techniques. These effects are more pronounced with the intraocular coils because of their small physical dimensions. Therefore, it is critical to understand the coil electrical properties with respect to its geometric design, as well as the relationship between coil dimensions and the power transfer efficiency of the system, the essential of which will be covered in this chapter.

3.2 Inductive link system overview

The all-intraocular retinal prosthesis system comprises an extraocular unit and an intraocular one. Power and data signal need to be transmitted from the extraocular unit to the intraocular unit for the stimulation of the retina and operation of all electronics. Our system relies on an inductive coupling link because it can provide the required power for a high-density retinal prosthesis and has relatively high efficiency compared with other power sources (Table 3.1). It also avoids permanent wired connections passing through the eyeball wall, minimizing undesired damages to eye tissues.

Table 3.1: Comparison of available power sources [63].

	Battery	Inductive	Infrared	Thermal
Transmitter	n/a	Coil	LED, Laser	Body heat
Receiver	n/a	Coil	Photodiode, phototransistor	Thermoelectric material
Available energy	Low	High	Moderate	Low
Efficiency	High	Moderate	Low	Low

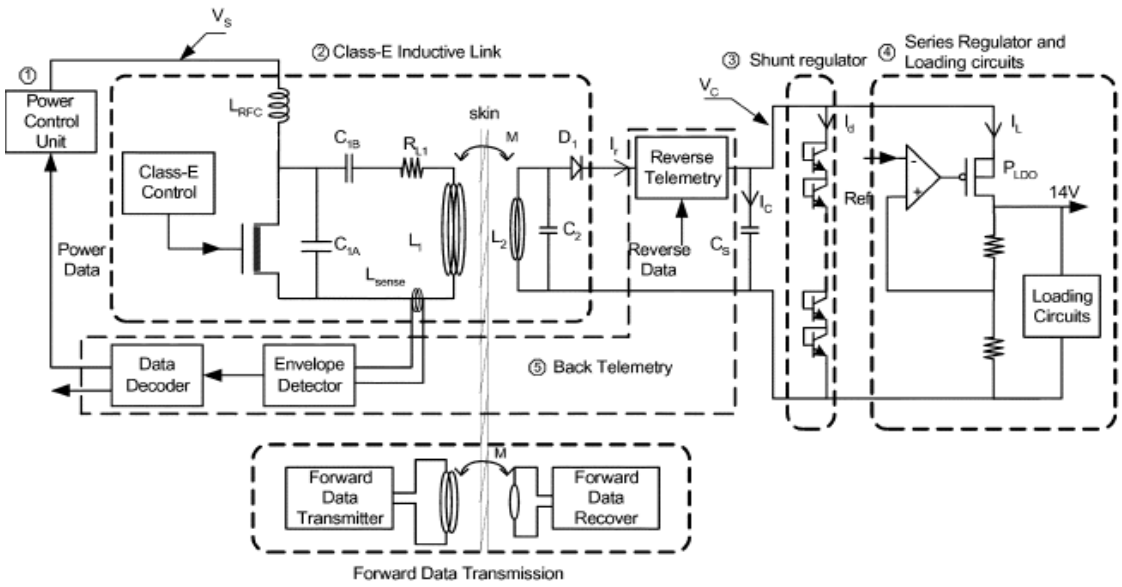


Figure 3.1: System configuration for the proposed system [64].

Inductive coupling is an established field and extensive research has been performed to analyze and optimize the operation of inductive links for biomedical applications [65-68]. In our approach, dual-band architecture with two pairs of coils is proposed (Figure 3.1) [64], which uses different frequencies to transmit data and power independently. The operation frequencies are predetermined according to human tissue absorption and circuit design constraints. Specifically, the data signal is modulated on a 20

MHz carrier at a data rate up to 2 Mbps, while the power transfer is performed at a frequency between 1 to 2 MHz. The minimum required power transferred through this inductive link is estimated to be ~ 100 mW in order to enable high-density stimulations and regular chip functions [69].

The inductive link design also needs to comply with the safety limit of electromagnetic energy deposition into human tissue, as the intraocular unit will be operated in human eyes. One of the most prominent biological effects induced by RF radiation is local hyperthermia, caused by the thermal energy through absorption. The attenuation rate of RF radiation in tissues varies over the frequency spectrum. Studies about the average specific absorption rate (SAR) over the whole body indicate that maximum energy absorption takes place between 30 and 100 MHz for human beings (Figure 3.2). It is also found that human eye is particularly susceptible to heat. Microwave radiation at frequencies above 800 MHz can cause injury to eye [70]. The inductive link used in our approach operates at frequencies lower than 20 MHz, where little energy absorption is expected.

The technical details of the inductive link circuitry are beyond the scope of this dissertation. The following sections will focus on the design procedures of MEMS receiver coils. A simplified inductive link model is also investigated to predict the power transfer capability of MEMS coils.

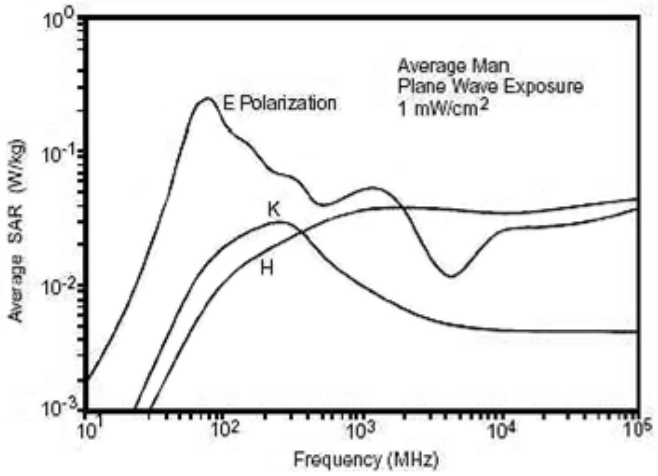


Figure 3.2: Average SAR for an average man exposed to 1mW/cm^2 plane wave. (E polarization denotes the electric field parallel to the body, H denotes the magnetic field parallel to the body and K denotes the wave moving from head to toes or toes to head.) [70]

3.3 Design of planar MEMS coils

In this section, we will concentrate on a circular shaped coil (Figure 3.3) to discuss the design procedure of a planar MEMS coil in general.

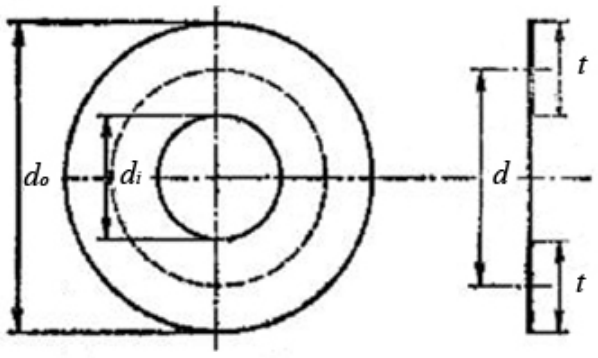


Figure 3.3: Simplified representation of a circular planar MEMS coil.

3.3.1 **Self-inductance**

The self-inductance of a coil, L_s, is defined as the magnetic flux linkage per unit current in the coil itself. In 1945, Dwight arrived at some expressions for self-inductance

of circular coils with rectangular cross-section [71]. For a single layer coil with only one turn, the self–inductance can be calculated using the following equation:

$$L_0 = 2\pi d \times 10^{-9}\left[\left(\ln\frac{4d}{t}\right)\left(1+\frac{t^2}{24d^2}\cdots\right)-\frac{1}{2}+\frac{43t^2}{288d^2}\cdots\right] \text{ (H)}, \qquad 3\text{-}1$$

where d (in cm) is the mean diameter of the coil and t (in cm) is the coil width, as given in Figure 3.3. If the coil has N layers of metal wires and n turns in each layer, its inductance will increase significantly due to mutual inductance.

$$L_s = 2\pi d(nN)^2 \times 10^{-9}\left[\left(\ln\frac{4d}{t}\right)\left(1+\frac{t^2}{24d^2}\cdots\right)-\frac{1}{2}+\frac{43t^2}{288d^2}\cdots\right] = (nN)^2 L_0 \text{ (H)}. \qquad 3\text{-}2$$

It can be seen that the self-inductance is determined by the coil dimensions. However, this expression holds true only if the coil is operated at low-frequency, i.e., no skin-effect.

3.3.2 **Effective series resistance**

The effective series resistance (ESR) of a planar MEMS coil, R_s, is used to estimate coil losses, which plays a significant role in designing a power efficient inductive link. In general, the ESR can be divided into two parts; one part is DC resistance and the other one is frequency dependent. For a single turn coil, its DC resistance can be calculated using Ohm's law, where ρ is the resistivity of the conductive material and h is the thickness of the metal wire.

$$R_0 = \rho \frac{\pi d}{t \times h} (\Omega). \quad 3\text{-}3$$

Assuming the width of metal traces is much larger than the space between adjacent turns which can be ignored, then the DC resistance of a coil with *N* layers of metal and *n* turns on each layer can be expressed as Equation 3-4.

$$R_s = \rho \frac{nN \times \pi d}{t/n \times h} = n^2 N R_0 \ (\Omega). \quad 3\text{-}4$$

The frequency dependent part, on the other hand, is caused by time varying magnetic fields produced by an alternating current passing through the conductor. This field can introduce eddy currents, which flow in the opposite direction to the applied currents. As a result, the current tends to shift to the surface of the wire, leading to an increase in the series resistance. This phenomenon is well known as "skin-effect", and the skin depth of a given conductor can be calculated by the following equation[72, 73], in which μ_0 is the permeability of free space ($4\pi \cdot 10^{-7} H/m$), μ_r is the relative permeability of conductive material, and ω is the angular frequency.

$$\delta = \sqrt{\frac{2\rho}{\omega \mu_0 \mu_r}} \ (\text{m}). \quad 3\text{-}5$$

In our retinal implants, we use gold wires ($\rho \sim 2.2 \times 10^{-8} \Omega \cdot m$ and $\mu_r \sim 1$) at frequencies ranging from 1 to 2 MHz. Therefore, the skin depth δ is calculated to be approximately 53 μm to 75 μm, which is by far greater than typical metal thicknesses deposited in an E-beam evaporator. Therefore the influence of the skin-effect is negligible and the coil ESR can be expressed using its DC resistance only (Equation 3-4).

3.3.3 **Parasitic capacitance**

Parasitic capacitance places a limit to the coil self resonant frequency, above which the coil will not behave as an inductor any more. The parasitic capacitance of a planar MEMS coil usually consists of three different capacitances: the capacitance between coil turns, the capacitance between layers, and the capacitance between the coil and substrate. In our case, silicon substrates will be completely removed, therefore only capacitances between turns and layers are considered. A distributed model is used to approximately estimate the equivalent parasitic capacitance [74]. In order to simplify this model, several assumptions are made:

1) The spacing between adjacent turns is much less than the width of metal traces, therefore it can be ignored.
2) The metal width and thickness are consistent everywhere so that voltage distribution is proportional to the lengths of metal traces.
3) Within the same turn, voltage is equally distributed, which is determined by averaging the beginning voltage and the ending voltage.
4) Only capacitances between adjacent turns and layers are taken into account. The capacitances between non-adjacent turns and layers are second order effects and will be neglected in this simplified model.

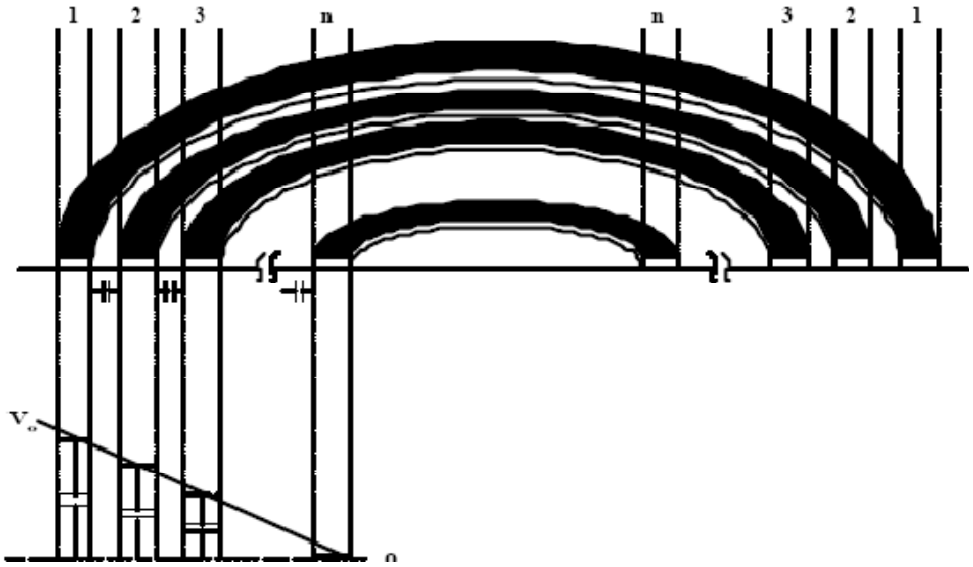


Figure 3.4: Voltage profile of an *n*-turn planar coil. [74]

Figure 3.4 shows voltage profile of a single layer coil with *n*-turn metal traces. The voltage in *k*-th turn can be express as Equation 3-6, where $d(k) \equiv h_1 + h_2 + ... + h_k$, and h_k is defined as the ratio of the wire length of the *k*-th turn (l_k) to the total wire length (l_{tot}).

$$V(k) = \frac{1}{2}[V(k)_{beg} + V(k)_{end}] = \frac{1}{2}V_0[2 - d(k-1) - d(k)]. \quad 3\text{-}6$$

Hence, the voltage drop between *k*-th and (*k*+1)-th can be derived as:

$$\Delta V(k, k+1) = V(k) - V(k+1) = \frac{1}{2}V_0[d(k+1) - d(k-1)]. \quad 3\text{-}7$$

The total reactive energy stored in the distributed capacitors can be expressed as:

$$E_{total} = \sum_{k=1}^{n-1}\frac{1}{2}C(k)\cdot\Delta V(k,k+1)^2 = \sum_{k=1}^{n-1}\frac{1}{2}C_{mm}l_k\cdot\frac{1}{4}\{V_0[d(k+1) - d(k-1)]\}^2, \quad 3\text{-}8$$

where C_{mm} represents the capacitance per unit length between adjacent metal turns. Based on the fact that this total reactive energy is equal to the energy stored in the equivalent lump capacitor, we can obtain the equivalent capacitance between adjacent turns by

$$C_{eq-t} = \sum_{k=1}^{n-1} \frac{1}{4} C_{mm} l_k [d(k+1) - d(k-1)]^2 \,. \qquad 3\text{-}9$$

A similar distributed model is applied to an *N*-layer stacked coil, where the voltage profile across the stacked layers is shown in Figure 3.5. The equivalent capacitance between adjacent layers is given as Equation 3-10:

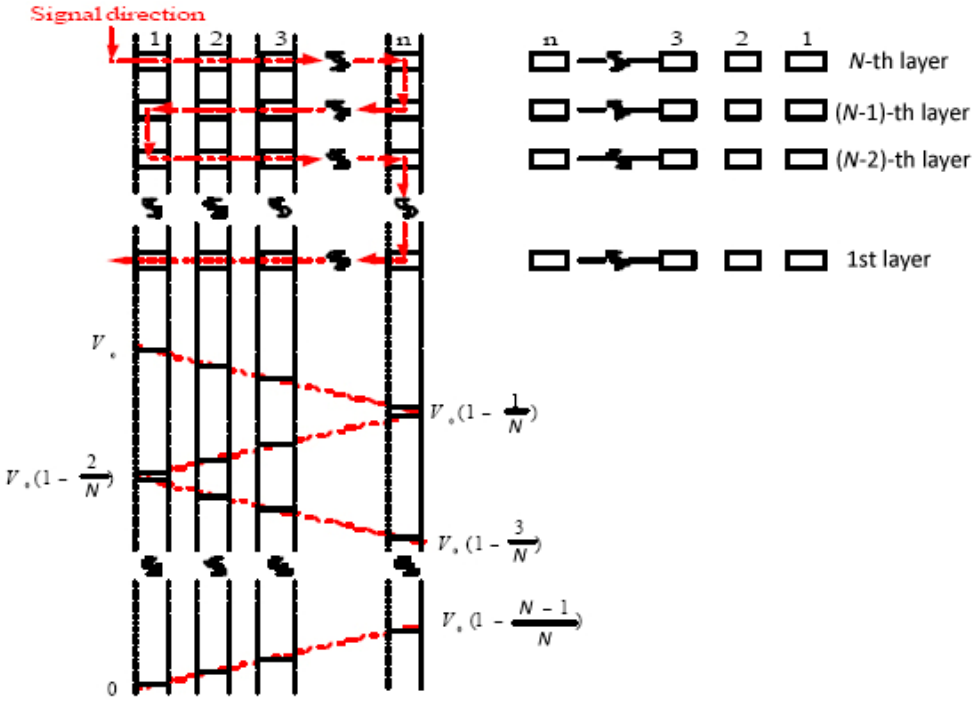


Figure 3.5: Voltage distribution of an *N*-layer coil.

$$C_{eq-l} = \frac{1}{4} \sum_{k=1}^{N} (C_{m,m-1} + C_{m-2,m-3} + \ldots) \frac{A_k}{m^2} [4 - 2d(k-1) - 2d(k)]^2 + \frac{1}{4} \sum_{k=1}^{N} (C_{m-1,m-2} + C_{m-3,m-4} + \ldots) \frac{A_k}{m^2} [2d(k-1) + 2d(k)]^2 \,, \qquad 3\text{-}10$$

where $C_{m,\ m-1}$ is the capacitance per unit area between the m-th and (m-1)-th metal layer, and A_k is the trace occupied area of the k-th turn. Therefore, the total parasitic lump capacitor is the sum of C_{eq-t} and C_{eq-l}.

3.3.4 **Self-resonant frequency and Quality factor**

The self-resonant frequency and quality factor (Q factor) of coils can be derived using an equivalent *RLC* model (Figure 3.6). The self-resonant frequency of this *RLC* tank is calculated as $\omega_s = \sqrt{\frac{1}{L_s C_s} - \frac{R_s^2}{L_s^2}}$. When $R_s << \sqrt{\frac{L_s}{C_s}}$, it can be simplified as $\omega_s \approx \sqrt{\frac{1}{L_s C_s}}$.

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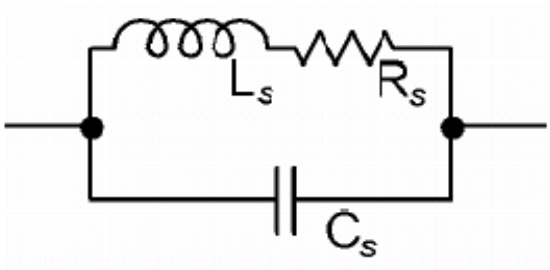


Figure 3.6: Equivalent *RLC* circuit of a MEMS coil.

Intrinsic quality factor (Q factor) is an important metric for evaluating the efficiency of a coil. Several definitions have been proposed for calculating the Q factor [75, 76]. In this work, we use the fundamental definition of Q factor, which is the ratio of total stored energy to dissipated energy per cycle in a resonating system. Therefore, the intrinsic Q factor can be expressed by Equation 2-11, where Z is the impedance of the coil.

$$Q_i = \frac{\mathrm{Im}(Z)}{\mathrm{Re}(Z)} \approx \frac{\omega_s L_s}{R_s}. \qquad 3\text{-}11$$

In order to achieve maximum couple energy, both the primary and secondary stages of the inductive link must be tuned to the same resonant frequency. Therefore, an extra capacitor has to be connected in parallel with the coil. Such tuning is possible only if the desired operation frequency is lower than the intrinsic resonant frequency of the coil. Assuming the resonant frequency is set as ω_0, and substituting L_s and R_s with Equations 3-2 and 3-4, the Q factor of the secondary coil can be modified as Equation 3-12, where L_0 and R_0 are the self-inductance and DC resistance of a single turn coil respectively.

$$Q_0 = \frac{\omega_0 N L_0}{R_0}. \qquad 3\text{-}12$$

It is obvious from above that the Q factor of the MEMS coil is independent of the number of turns on each layer. To enhance the Q factor, there are several methods: to increase the number of coil layers N, to increase L_0, or to reduce R_0. For the intraocular retinal implant, however, there is not much room to improve L_0 because the coil dimensions (inner diameter, outer diameter, etc.) are confined by the eyeball size. Therefore, the improvement of the Q factor has to rely on the increment of the number of layers, as well as the thickness of metal which determines the DC resistance R_0.

3.3.5 **Simulation results**

To evaluate the theoretical models described above, finite element simulations are performed using a built-in package in CoventorWare (Coventor Inc., Cary, NC). A coil with two layers of metal is designed, and its electrical characteristics are calculated using theoretical models, as summarized in Table 3.2. The thickness of the insulation layer

between two metal layers is set to 4 μm, which can vary slightly depending on fabrication processes.

Table 3.2: Design specifications of a sample coil.

OD (mm)	ID (mm)	Trace cross section (μm × μm)	Number of turns	L_s (μH)	R_s (Ω)	C_s (nF)	Q at 1MHz
10	3	220 × 2	28 / Layer	5	28.9	65.5	1.1

(OD: outer diameter. ID: inner diameter)

Finite element analysis is done to simulate the self-inductance and the ESR over a frequency range from 10 kHz to 1 GHz using the same coil geometries from Table 3.2 (Figure 3.7). Due to the memory constraint of CoventorWare, an octagonal coil is used in the simulation instead of a circular one. Figure 3.7 shows that the simulation results match the calculated values very well. The self-inductance at 1 MHz shows 2.2% deviation, and the ESR deviates by 5.5%. These errors might be introduced by the approximation of coil shape. L_s, and R_s both remain stable at frequencies below 10 MHz, indicating that skin effect or proximity effect is negligible at target frequencies of 1 or 2 MHz.

L_s, R_s and Q factor associated with the number of turns on each layer have also been investigated, as shown in Figure 3.8. In this case, the coil ID and OD remain the same, while the number of turns decreases and the width of metal traces increases from 220 μm to 660 μm. It can be seen that L_s and R_s increase as the number of turns increases, while the Q factor of the coil at 1 MHz does not show much change. This result indicates the Q factor is independent of the number of turns on each layer, which is consistent with our theoretical prediction (Equation 3-13).

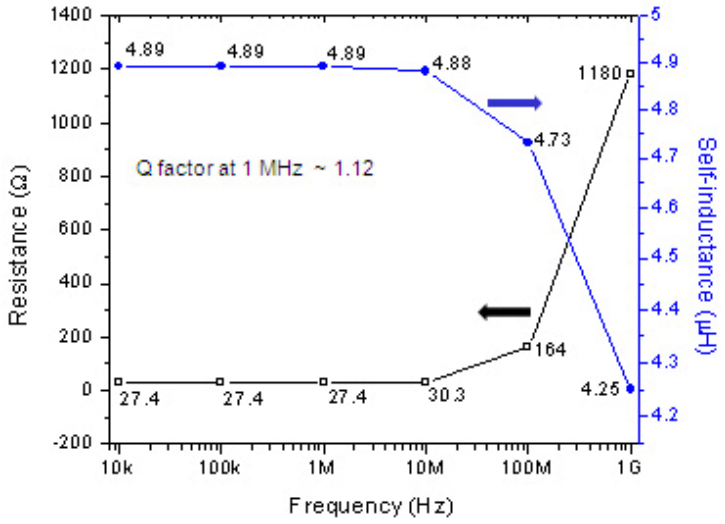
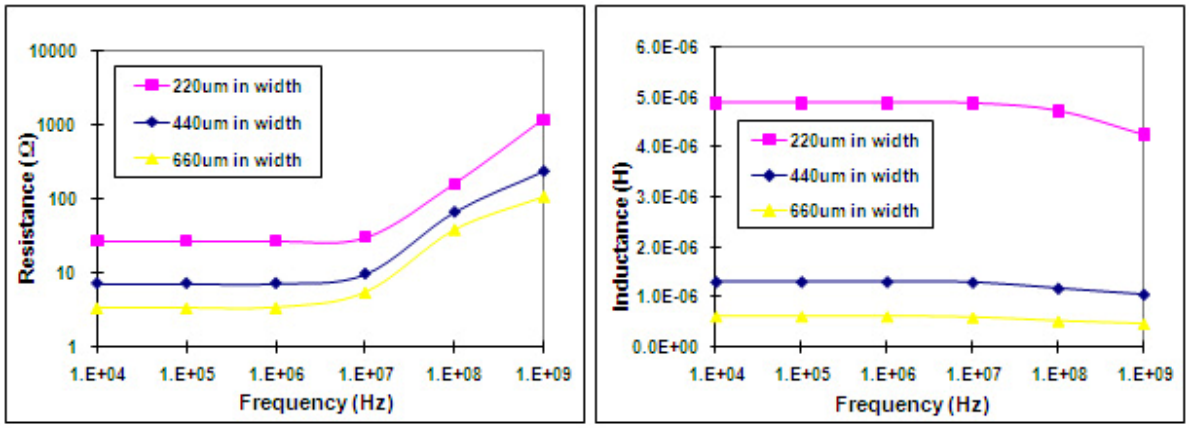


Figure 3.7: Simulated self-inductance and ESR of the sample coil. (Simulation courtesy of Dr. Wen-Cheng Kuo.)



Line width (um)	220	440	660
Q factor at 1 MHz	1.12	1.16	1.16

Figure 3.8: Simulated self-inductances and ESR as functions of trace widths. The Q-factors are summarized in the table. (Plots courtesy of Dr. Wen-Cheng Kuo.)

3.4 Inductive power link

In order to estimate the power transfer capability of the MEMS coil, a simplified inductive powering circuit is built (Figure 3.9). In this model, the load of the implanted

electronics to which power is delivered is represented by R_L. The rectifier is modeled with a diode D_1 and C_L. The lossy transmitter coil is modeled with an ideal inductance L_1 and an ESR (R_1). Similarly, the receiver coil is modeled with L_2 and R_2. The parasitic capacitors of the coils and the tuning capacitors are combined together as C_1 and C_2.

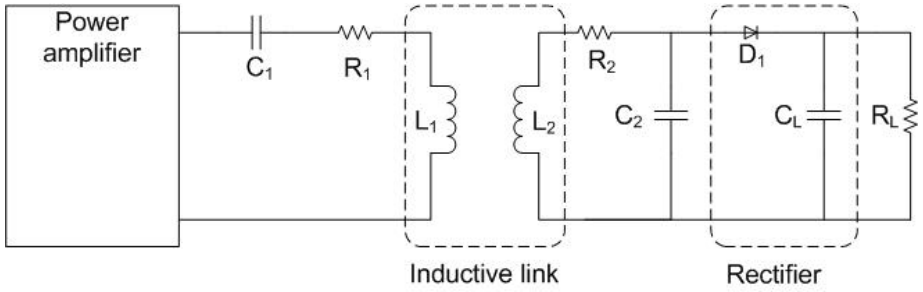


Figure 3.9: System overview of an inductive power link for biomedical applications. The secondary stage is modeled as a nonlinear circuit.

Analysis of this model is not trivial due to the nonlinearity of the rectifier. Therefore, we can converted it into a linear model by transfer the DC load into an AC equivalent linear load, as shown in Figure 3.10 [77].

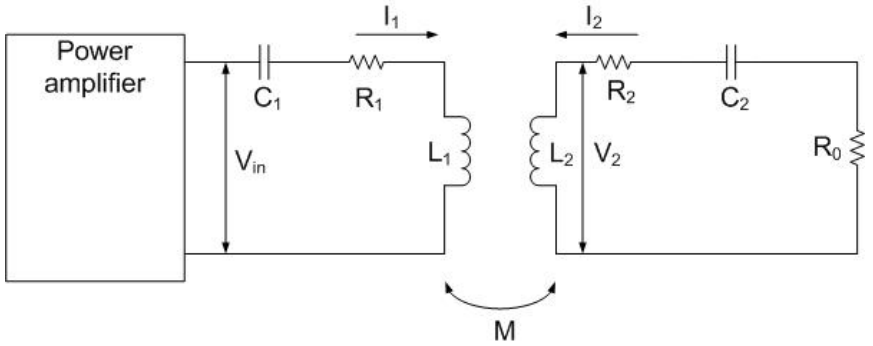


Figure 3.10: The secondary stage is simplified with an approximated linear model.

By maintaining the power dissipation equivalent to the DC power in R_L, the AC equivalent load can be expressed by Equation 2-13.

$$R_0 = \frac{1}{\omega^2 C_2^2 R_L / 2} = \frac{2\omega^2 L_2^2}{R_L}. \quad 3\text{-}14$$

This approximation holds true only when the peak AC voltage across the L_2C_2 tank exceeds several volts and $C_L R_L \gg \frac{1}{f}$, so that the voltage drop across the diode can be neglected.

With current direction defined as in Figure 3.10, the voltage drop across each terminal can be express as the following equations because of the magnetic coupling effect between two coils [78]:

$$V_{in} = I_1(R_1 + \frac{1}{j\omega C_1} + j\omega L_1) + j\omega M I_2, \quad 3\text{-}15$$

$$V_2 = j\omega L_2 I_2 + j\omega M I_1 = -I_2(R_2 + R_0 + \frac{1}{j\omega C_2}), \quad 3\text{-}16$$

V_{in} is the AC output voltage from the power amplifier, and V_2 is the AC voltage across the secondary coil. M is the mutual inductance, associated with L_1 and L_2 by coupling coefficient, and is defined as:

$$M = k\sqrt{L_1 L_2}. \quad 3\text{-}17$$

Assuming that the primary and secondary stages are both tuned to the same resonant frequency $\omega = \frac{1}{\sqrt{L_1 C_1}} = \frac{1}{\sqrt{L_2 C_2}}$, the relationship between I_1 and I_2 can be derived, as the following equation.

$$\frac{I_2}{I_1} = -\frac{j\omega M}{R_2 + R_0} = -k\sqrt{\frac{L_1}{L_2}}\frac{j\omega I_2}{R_2 + R_0}. \quad \text{3-18}$$

Combine Equations 2-14, 2-15 and 2-17, we can obtain the equivalent resistance reflected back into the primary coil due to magnetic coupling link as:

$$R_e = \frac{\omega^2 M^2}{R_2 + R_0}, \quad \text{3-19}$$

and the ratio of V_0 over V_{in} is:

$$\frac{V_0}{V_{in}} = \frac{-I_2 R_0}{I_1 R_1 + \frac{\omega^2 M^2}{R_2 + R_0} I_1} = \frac{j\omega M R_0}{R_0 R_1 + R_2 R_1 + \omega^2 M^2}. \quad \text{3-20}$$

Then, the overall voltage gain of this inductive link can be calculated by keeping the same power consumption between the AC load and DC load, as shown in Equation 2-8.

$$G_v = \frac{V_{out}}{V_{in}} = \frac{V_0}{V_{in}}\sqrt{\frac{R_L}{R_0}} = \frac{j\sqrt{2}\omega^2 M L_2}{\frac{2\omega^2 L_2^2}{R_L} R_1 + R_2 R_1 + \omega^2 M^2}. \quad \text{3-21}$$

The total power transfer efficiency of the inductive link, defined as the ratio between the power delivered to the load and the output power from the power amplifier, is expressed as:

$$\frac{P_{out}}{P_{in}} = \frac{P_0}{P_{in}} = \frac{\frac{1}{2}|V_0 I_0|}{\frac{1}{2}|V_{in} I_1|} = \frac{R_e}{R_e + R_1}\frac{R_0}{R_0 + R_2} = \frac{\omega^2 M^2 R_0}{R_1(R_2 + R_0)^2 + \omega^2 M^2 (R_2 + R_0)}$$
$$= \frac{2\omega^4 k^2 L_1 L_2{}^3 R_L}{(R_L R_2 + \omega^2 L_2{}^2)(R_L R_1 R_2 + 2\omega^2 L_2{}^2 R_1 + \omega^2 k^2 L_1 L_2 R_L)}. \quad 3\text{-}22$$

The power lost in the receiver coil (P_{R1}) is determined by the coil ESR, and the ratio of P_{R1} over P_{in} can be calculated by:

$$\eta_{lost} = \frac{P_{R1}}{P_{in}} = \left|\frac{I_2^2 R_2}{V_2 I_2}\right| = \frac{\omega^2 M^2 R_2}{R_1(R_2 + R_0)^2 + \omega^2 M^2 (R_2 + R_0)}$$
$$= \frac{\omega^2 k^2 L_1 L_2 R_2 R_L^2}{(R_2 R_L + 2\omega^2 L_2^2)(R_1 R_2 R_L + 2\omega^2 L_2^2 R_1 + \omega^2 k^2 L_1 L_2 R_L)}. \quad 3\text{-}23$$

As described in the previous section, L_2 and R_2 are functions of receiver coil dimensions. The coupling coefficient, denoted by *k*, is also a function of coil geometry. It is known that the coupling coefficient has a relationship with the mutual inductance, we can obtain *k* from Equation 3-17 [77].

$$k^2 = \frac{M^2}{L_1 L_2} = \frac{(1.27N^*)^2}{F_1 \cdot F_2}, \quad 3\text{-}24$$

where F_1 and F_2 are the shape factors for the primary and secondary coil, and N^* is a function of $\frac{r_2}{r_1}$ (Figure 3.11) with the ratio $\frac{r_2}{r_1}$ to be determined as:

$$\frac{r_2}{r_1} = \sqrt{\frac{(d_1 - d_2)^2 + 4D^2}{(d_1 + d_2)^2 + 4D^2}}. \quad 3\text{-}25$$

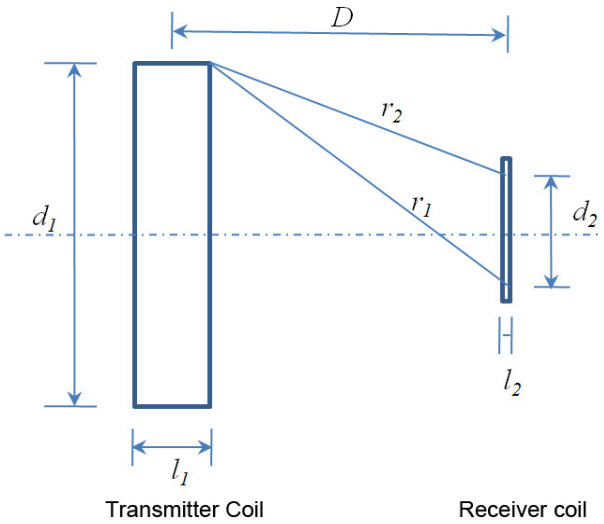


Figure 3.11: Depiction of the inductive link, showing the size and relative position of the transmitter coil and receiver coils.

The values of F_2 and N^* as a function of $\frac{r_2}{r_1}$ can be found in '*Radio Engineers Handbook*' [79], while F_2 can be calculated by $2\pi\times10^{-10}\left[\left(\ln\frac{4d_2}{t_2}\right)\left(1+\frac{t_2^{\,2}}{24d_2^{\,2}}\cdots\right)-\frac{1}{2}+\frac{43t_2^{\,2}}{288d_2^{\,2}}\cdots\right]$. These factors are all independent of the number of turns if the coil geometries are already known. Therefore the coupling coefficient is unrelated to the number of turns of the coils. It should be noted here that the N^* increases as $\frac{r_2}{r_1}$ decreases, therefore, to achieve maximum *k*, minimum $\frac{r_2}{r_1}$ is desired. By setting $d(\frac{r_2}{r_1})/d(d_1)$ to zero, we can optimize the design of the transmitter coil d_1 with given d_2 and D, as shown in the following equation.

$$d_1=(d_2^2+4D^2)^{1/2}. \qquad \text{3-26}$$

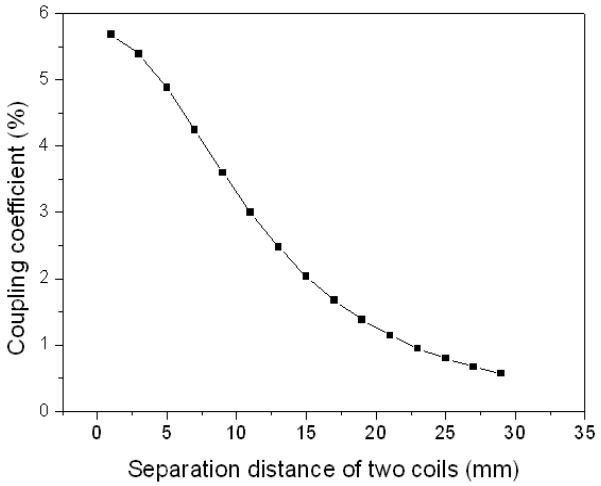


Figure 3.12: Coupling coefficient as a function of coil separation (Transmitter coil ~ 30.8 mm in OD. Receiver coil ~ 9mm in OD).

In the retinal prosthesis, for example, given an inner diameter of 5 mm and an outer diameter of 9 mm for the receiver coil, and the coil separation of approximately 15 mm, we can optimize the diameter of the primary coil to be ~ 30.8 mm. Therefore, the relationship between the coupling coefficient and the coaxial separation distance of the coil pair can be obtained as shown in Figure 3.12. At the separation distance of 15 mm, the maximum coupling efficiency is calculated to be ~ 2.03%. This value matches the measured number (~ 2%) from Prof. Wentai Liu's group at the University of California, Santa Cruz (UCSC), where a primary coil with a diameter of ~ 28 mm is used [80].

Based on the analysis described above, and given the parameters of the load and transmitter coil, the voltage gain and power gain of the inductive link can be rewritten as functions of the physical geometries of the receiver coil, by substituting L_2 and R_2 with Equations 3-2 and 3-4.

$$G_v = \frac{j\sqrt{2}\omega^2 k\sqrt{L_1 L_{20}}\, n_2 N_2^2 L_{20}}{\frac{2\omega^2 n_2^2 N_2^3 L_{20}^2}{R_L} R_1 + R_1 R_{20} + \omega^2 k^2 L_1 N_2 L_{20}}, \quad 3\text{-}27$$

$$\eta = \frac{P_{out}}{P_{in}} = \frac{2\omega^3 k^2 Q_1 n_2^2 N_2^4 L_{20}^3 R_L}{(R_{20}R_L + 2\omega^2 n_2^2 N_2^3 L_{20}^2)(R_{20}R_L + 2\omega^2 n_2^2 N_2^3 L_{20}^2 + \omega k^2 Q_1 N_2 L_{20} R_L)}, \quad 3\text{-}28$$

$$\eta_{lost} = \frac{P_{R1}}{P_{in}} = \frac{k^2 Q_1 Q_2 R_L^2}{(R_L + 2\omega n_2^2 N_2^2 L_{20} Q_2)(R_L + 2\omega n_2^2 N_2^2 L_{20} Q_2 + k^2 Q_1 Q_2 R_L)}, \quad 3\text{-}29$$

where N_2 is the number of layers, n_2 is the number of turns on each layer, L_{20} and R_{20} are the self-inductance and ESR of the single turn coil expressed by Equations 3-1 and 3-3, respectively.

Analytical simulations have been done using MATLAB (The MathWorks, Natick, MA). The transmitter coil has a self-inductance of 69 μH and an ESR of 3.7 Ω. The DC load R_L is approximately 1024 Ω. These parameters are adopted from [67] to meet the specifications of UCSC's system. The receiver coil used in the retinal implant has an outer diameter of 9 mm and an inner diameter of 5 mm, predetermined based on medical experiments performed at USC. The metallization of the receiver coil consists of 2 μm thick gold traces, which is typical of what we can get from our e-beam evaporator. The coupling efficiency is approximately 2.03% according to a separation distance of around 15 mm, which is limited by the implantation depth. The voltage and power gains as functions of N_2 and n_2 are calculated, as plotted in Figure 3.13. Given the number of turns per layer, a coil has an optimal power transfer efficiency and voltage gain associated with a certain number of layers. Coils with less number of turns on each layer potentially have higher

maximum voltage and power gain than those with more number of turns. This simulation provides us a guideline when we design the coil.

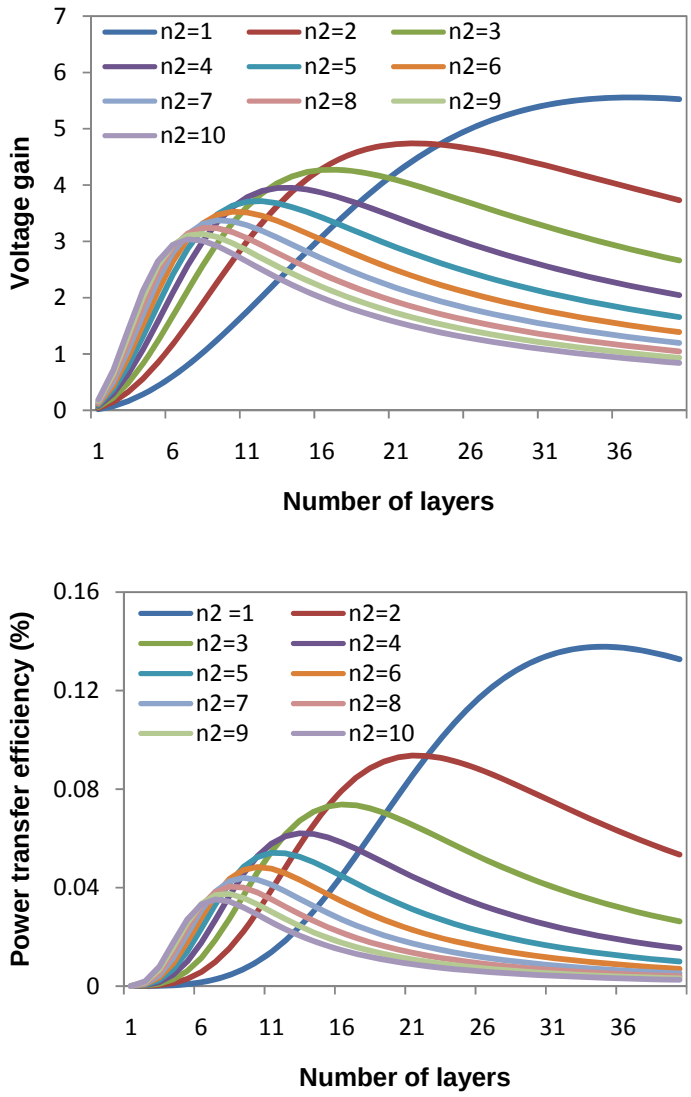
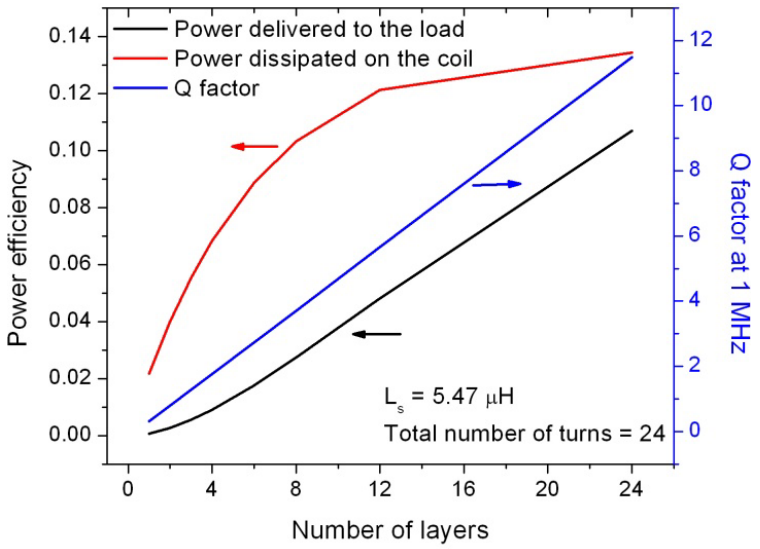


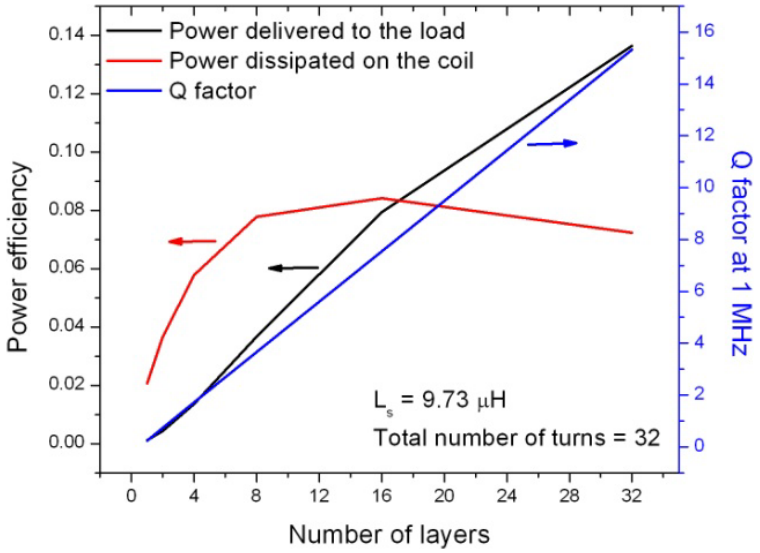
Figure 3.13: Analytical simulations of voltage gain (*top*) and power gain (*bottom*) as functions of the receiver coil geometries. (n2 denotes the number of turns per layer.)

In the simulation, there is no constraint in term of the coil inductance. However, in the real inductive link circuit, the inductance must be designed within a reasonable range such that the coil self-resonant frequency is well above the operation frequency. For the

receiver coil used in our system, an initial estimation of self-inductance is between 5 and 10 μH. With a fixed self-inductance, the power transferred to the load and the power dissipated in the receiver coil are investigated with respect to the coil geometries, as shown in Figure 3.14. The results show that the power transfer efficiency increases as the Q factor of the receiver coil goes up. The trend of power dissipations suggests a maximum value at a certain Q factor, depending on the self-inductance of the receiving coil. When the Q factor is low, the power dissipated in the coil ESR is much higher than the power delivered to the load. As the Q factor increases, the dissipated power becomes comparable to or even lower than delivered power, implying that the overall efficiency is improved. Given the same Q (i.e., same number of layers), the coil with a higher self-inductance has less power loss, and thus a better overall efficiency of the inductive power link [67].



(a)



(b)

Figure 3.14: Power delivered to the load, power dissipation and coil Q factors vs. number of layers. (a) Coil with an inductance of 5.47 μH. (b) Coil with an inductance of 9.73 μH.

3.5 Summary

The electrical properties of MEMS receiver coils, including self-inductance, ESR, and parasitic capacitance, are predicted with respect to the coil geometries using analytic models. The calculation values are consistent with the simulation results in CoventorWare. We have also studied a simplified inductive link to evaluate the power transfer capability of MEMS coils. The result indicates that a higher Q factor will improve the transfer efficiency and overall efficiency of the inductive link. Due to the nonlinear nature of the system, more accurate analysis may be needed in the future to simulate the circuit characteristics under nonlinear conditions using SPICE [67]. Nevertheless, the theoretical analysis above provides us a better understanding of the parasitic effects of the MEMS coil, and gives us the possibility to optimize the coil geometries to achieve maximum power transfer efficiency.

Chapter 4 IMPLANTABLE MEMS RF COIL FOR POWER AND DATA TRASMISSION

4.1 Introduction

Following the theory on coil design in the previous chapter, this chapter will describe the design, fabrication, and measurements of two types of implantable and flexible MEMS coils as receiver coils in the retinal implant system. The coils are fabricated based on the Parylene-metal-Parylene skin technology described in Section 2.2 . Preliminary test results of power and data coupling effects are discussed and compared with theoretical predictions.

4.2 Planar MEMS RF coil

4.2.1 Design and fabrication

The first approach we have proposed is a planar MEMS coil, featuring thin-film metal conductive wires sandwiched between multiple layers of Parylene C. Parylene C serves as a substrate material as well as an insulating material. The interconnection between two adjacent layers is implemented with a through hole in the Parylene insulation layer. To form a closed path with two perimeter contacts, at least two layers of metal are needed. Figure 4.1 depicts a typical structure of a dual-metal-layer MEMS RF coil.

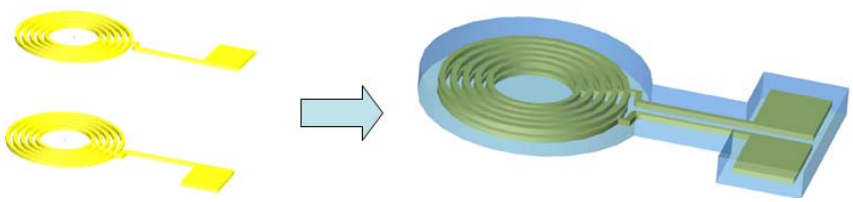


Figure 4.1: Schematics of a dual-metal-layer MEMS coil.

The detailed fabrication process for making such a dual-metal-layer coil is illustrated in Figure 4.2. First, a layer of sacrificial photoresist is optionally spun on a standard silicon wafer, followed by a ~5 µm Parylene C deposition. Then, an approximately 2000 Å layer of gold, with optional titanium adhesion layers 250 Å thick, is deposited and patterned using a wet etching process. After that, approximately 2 µm of Parylene C is deposited as an insulation layer, and patterned with oxygen plasma to open the interconnection vias between the two layers of metal. Another layer of metal is then deposited and patterned, followed by Parylene deposition so that the metal wires are entirely encapsulated. A photoresist mask is then patterned to expose the contact pads, as well as to define the coil profile. Finally, oxygen plasma is performed again to remove unwanted Parylene, and the entire flexible device is released from the silicon substrate.

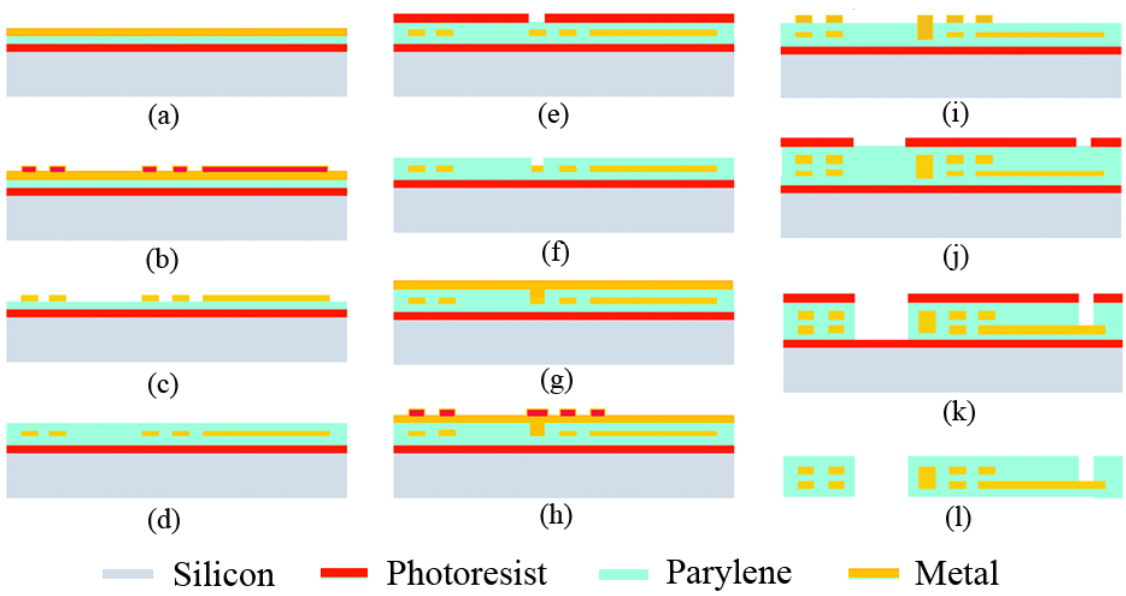


Figure 4.2: Detailed process of Parylene-based MEMS coil fabrication.

The reliability of the interconnection between metal layers highly depends on the step coverage of the Parylene sidewall during metal evaporation, which can be improved by a slightly isotropic O_2 plasma etch [81]. A special design of rotating wafer holder inside the e-beam evaporator also helps to adjust the angle of attack of metal evaporant for best coverage. Coils comprising more than two layers of metal can be also fabricated with this technology by alternating the Parylene deposition, interconnection via fabrication, and metal evaporation process steps. Although it is specifically developed for coil fabrication, this technology can be used for making other flexible devices with multi-layer metal as well, such as dual-metal-layer electrode arrays [82].

4.2.2 **Fabrication results**

A fabricated coil prototype is shown in Figure 4.3(a), and Figure 4.3(b) shows a magnified view of the interconnection via between the two layers of metal. This coil prototype has 10 turns of metal wires in total with multiple layers of Ti/Au/Ti metallization. Titanium is involved as an adhesion layer to improve the bonding strength between gold and Parylene C. Because of the downscaling nature of MEMS technologies, this microfabricated device has relatively small dimensions of 9.5 mm in outer diameter, 5 mm in inner diameter, and approximately 11 μm in total thickness. The interconnection via has a contact area of ~ 0.056 mm^2, resulting in a contact resistance less than 1 Ω, which is negligible compared with the coil ESR. The device is proven to be flexible and foldable (Figure 4.4), facilitating the surgical procedure as well as alleviating mechanical damages in the region of implantation. Although the coil dimensions are specifically designed for

the needs of intraocular retinal prostheses, the geometries can be easily modified depending on application requirements.

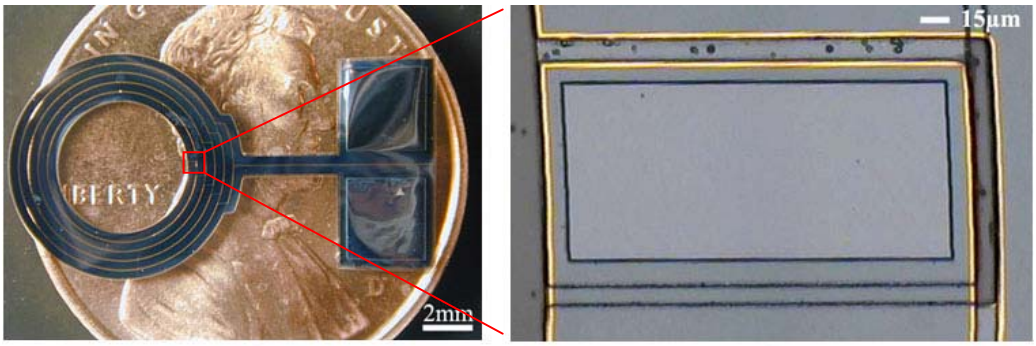


Figure 4.3: A fabricated ocular coil sitting on a penny. The right microscope image shows the interconnection via between two layers of metals.

Figure 4.4: Demonstration of coil flexibility and foldability.

4.2.3 **MEMS coil characteristics**

For a planar MEMS coil, there is no trivial way to directly measure its electrical characteristics due to the existence of parasitic elements. As we mentioned in Section 3.3.4 , the coil can be characterized using a simplified equivalent circuit (Figure 4.5), in which an inductor (L_s) and a resistor (R_s) in series account for the coil self-inductance and ESR, and a parallel capacitor (C_s) accounts for the capacitive coupling between metal lines and different layers of metal. Therefore, the total coil impedance of the equivalent circuit can be written as the sum of a real part and an imaginary part.

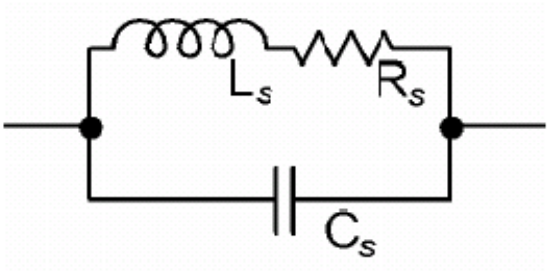


Figure 4.5: Equivalent *RLC* circuit of a MEMS coil.

$$Z_s = \frac{R_s}{(1-\omega^2 L_s C_s)^2 + (\omega C_s R_s)^2} + j\frac{\omega(L_s - R_s{}^2 C_s - \omega^2 L_s{}^2 C_s)}{(1-\omega^2 L_s C_s)^2 + (\omega C_s R_s)^2}. \quad 4\text{-}1$$

Two relationships can be derived by setting the derivative of the real part to zero and equating the imaginary part to zero:

$$2\omega_0^2 L_s^2 C_s - 2L_s + R_s{}^2 C_s = 0, \quad 4\text{-}2$$

$$L_s - R_s{}^2 C_s - \omega_z{}^2 L_s{}^2 C_s = 0. \quad 4\text{-}3$$

Frequency ω_0 is defined as the frequency at which the real part of the impedance is maximum, and the zero-reactance frequency ω_z is defined as the frequency at which the imaginary part of the impedance is zero. In the equivalent circuit, the ESR of the coil (R_s) is the DC resistance, which can be easily measured. Two important frequencies ω_0 and ω_z can be obtained by measuring the frequency dependent impedance of the coil. Knowing R_s, ω_0 and ω_z, the self-inductance L_s and the parasitic capacitance C_s can be extracted using Equations 4-4 and 4-5.

$$L_s = \frac{R_s}{\sqrt{2(\omega_0^2 - \omega_z^2)}}, \quad 4\text{-}4$$

$$C_s = \frac{\sqrt{2(\omega_0{}^2 - \omega_z{}^2)}}{R_s(2\omega_0{}^2 - \omega_z{}^2)}. \quad 4\text{-}5$$

This 3-element model is then used to analyze the fabricated coil and to determine its electrical characteristics. The I-V curve of the coil is first measured with an HP 4145B semiconductor parameter analyzer, as shown in Figure 4.6. The DC resistance is calculated to be 72 Ω with a gold resistivity of approximately 2.25×10^{-6} Ω·cm. This value matches the resistivity of bulk gold (2.2×10^{-6} Ω·cm), implying that the E-beam evaporated metal is void-free.

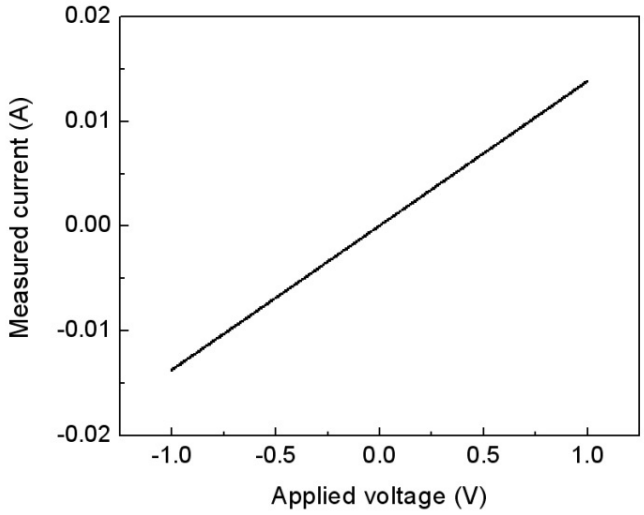


Figure 4.6: Typical I-V curve of the Parylene-based coil.

The coil impedance is then measured with an HP 4192A LF impedance analyzer over a frequency range from 5 Hz to 13 MHz. From the impedance versus frequency curves (Figure 4.7), f_0 and f_z can be read with values of 7.5 MHz and 3.3 MHz respectively. Therefore, L_s and C_s can be calculated as L_s = 1.19 μH and C_s = 201 pF.

The theoretical numbers are also calculated using the equations described in Chapter 2, and a fitting curve is plotted in Figure 4.7 to compare with the measured curve. It can be seen that the measured curve matches theoretical calculations closely with slight deviations. The errors may be attributed to the simplification of the 3-element model and measurement errors. The Q factor of the microfabricated coil is calculated to be approximately 0.1 at the target frequency of 1 MHz, as expected from the design.

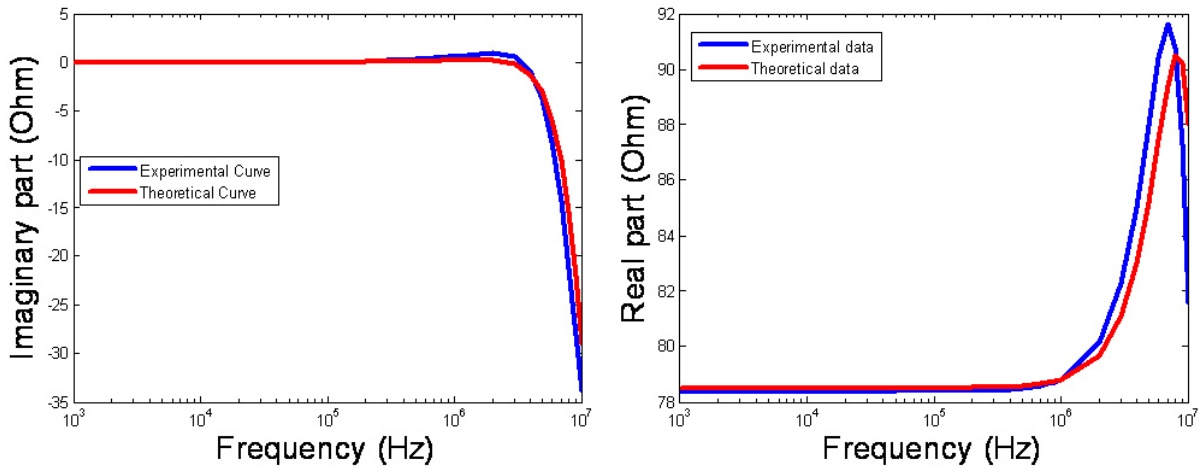


Figure 4.7: Coil impedance measurement and curve fitting using the 3-element model: (*right*) Imaginary part; (*left*) Real part. (Data correspond to electrical parameters of coil in Figure 4.3, L_s = 1.19 μH, R_s = 72 Ω and C_s = 201 pF).

4.2.4 **Data and power transfer measurements**

The data transfer behavior is tested using a data link designed by Dr. Wentai Liu's group at UCSC, as shown in Figure 4.8. The hand-wound primary coil has 4 turns of wire with a self-inductance of approximately 1 μH. The test waveforms are shown in Figure 4.9, in which the blue curve represents the data driving signal on the primary stage, the green curve represents the voltage across the primary coil, and the purple curve represents the receiving voltage across the secondary coil. The results show that the data signal can

be successfully transmitted through the MEMS coil. It is also noticed that the detectable signal level of the MEMS coil is less than that of a discrete hand-wound coil, indicating that larger transmission signal would be required on the primary stage. This is mainly limited by the low inductance and the small Q factor (0.1) of the receiver coil.

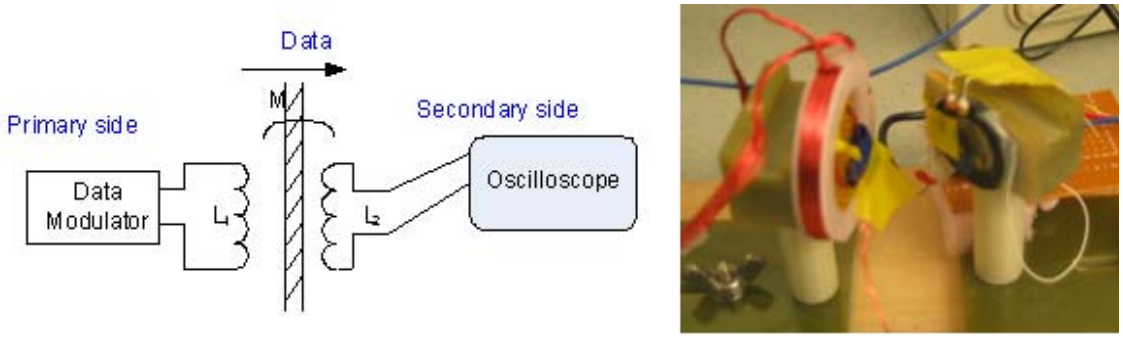


Figure 4.8: Schematic of the experimental setup for data transmission measurement. (Images courtesy of Dr. Wentai Liu)

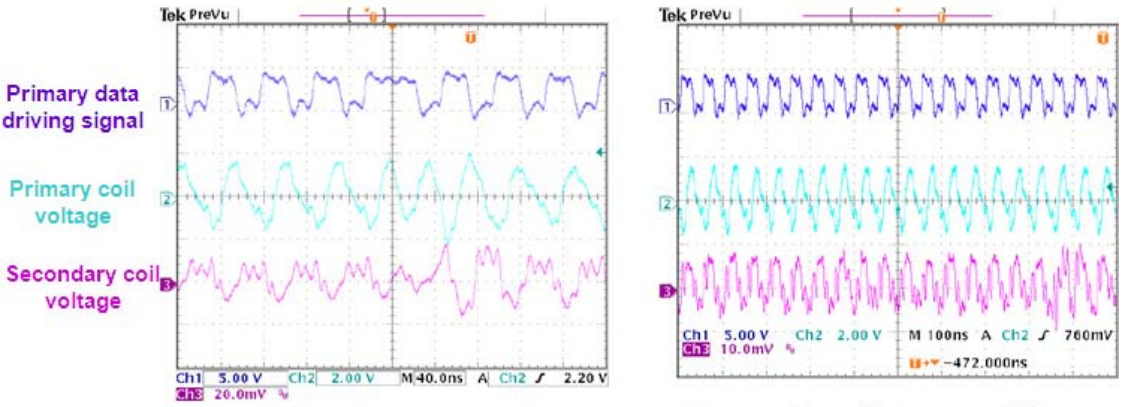


Figure 4.9: Inductive coupling test waveforms: (*left*) received signal is 25 mV peak to peak; (*right*) received signal is 15 mV peak to peak. (Plots courtesy of Dr. Wentai Liu)

The power transfer effect is also measured using the same coil at UCSC. However, it is found that the coil has no driving capability due to the small Q-factor, meaning that the power cannot be delivery to the load. Therefore, it is necessary to build high-Q coils in order to achieve high power transfer efficiency. Experiments have been done at UCSC to

study the feasibility of using MEMS coils as the receiver coil for the current inductive link design. A rough estimate is that, in the worst case, a minimal Q-factor of 10 is needed in order to deliver ~100 mW for chip operation and stimulation [80]. From Chapter 3, we know that the Q-factor can be enhanced by increasing the metal thickness and/or the number of metal layers. However, e-beam evaporated metals are usually limited in film thickness due to process cost. Electroplated and sputtered metals can be thicker alternatives but their qualities, such as density and conductivity, are typically not as good as evaporated metals. This concern becomes more crucial especially when devices are implanted inside harsh biological environments. Therefore, increasing metal layers is more practical for the Q factor enhancement of MEMS coils, and a fold-and-bond technology emerges as a good candidate [83].

4.3 Fold-and-bond MEMS coil

4.3.1 **Introduction**

In the concept of fold-and bond technology as depicted in Figure 4.10, two or more thin-film planar spiral coils are fabricated from the same batch so that each single coil has identical self-inductance and ESR, denoted by L and R respectively. Accordingly, a new coil can be formed by stacking n single coils together in either parallel or series connections. For parallel stacking, the new coil will have identical inductance but n times larger in equivalent metal thickness, resulting in an n times lower ESR. As for series stacking, the resistance remains the same while the inductance increases by n times because of the mutual inductance between different layers. According to the definition of the Q factor (refer to Section 3.3.4), both approaches can achieve an n-fold Q factor

enhancement. In this dissertation, fold-and-bond coils are fabricated using the series stacking approach to demonstrate the technology concept.

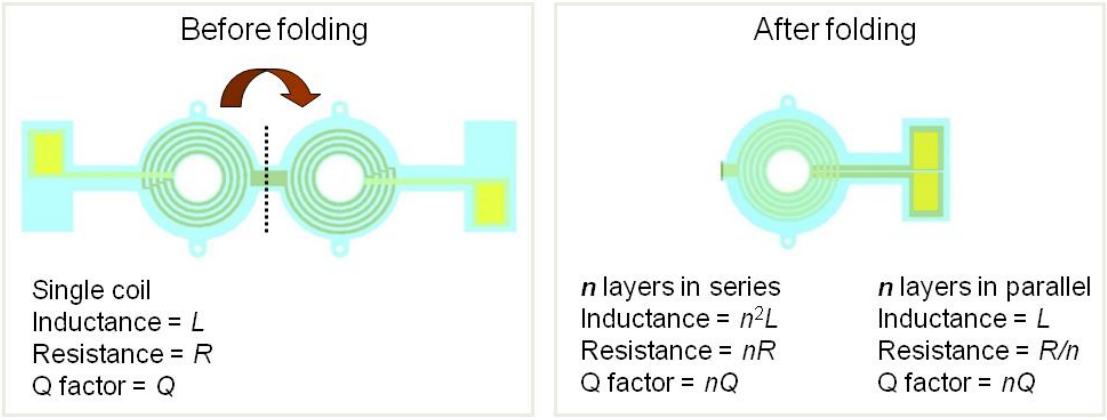


Figure 4.10: Concept of fold-and-bond technology for Q-factor enhancement. A coil with one fold is depicted for representation.

4.3.2 **Fabrication**

The fold-and-bond coil technology requires the dual-metal-layer Parylene/metal skin realization and a post-fabrication thermal bonding process. Briefly, a Parylene-based skin with two buried layers of metal is first made, in which one layer of metal is used for building the conductive wires of the coil, while the other layers is used for making the interconnections between the layers. This thin film skin is then folded and stacked into multiple layers thank to the flexibility of Parylene C. After that, the folded skin will be annealed in a vacuum oven, and consequently the separated layers can be bonded together into a whole piece.

Two prototypes of Parylene-based skins with two layers of metal have been designed and fabricated in the same manner as in Section 4.2.1 . The thickness of metal

wires is increased to ~2 μm in order to further reduce coil DC resistance. The metal is covered with ~3.4 μm Parylene C on each side with the lead contact vias open.

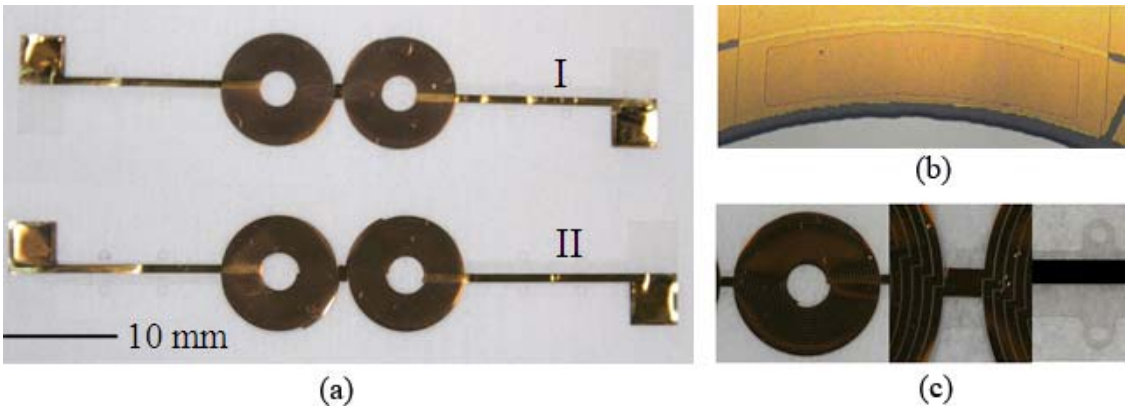


Figure 4.11: (a) Fabricated dual-metal-layer Parylene-based skins; (b) Microscope image of an interconnection via between two metal layers; (c) Photos of device details (From left to right): conductive wires of the coil, folding junction and suturing holes.

After the coil skins are fabricated, a thermal bonding process is performed to fuse the separate layers together. Preliminary bonding tests are conducted to find out the optimal bonding condition between Parylene layers. During the tests, the Parylene-based skins are folded and stacked together with the assistance of two glass slides. Aluminum sheets are inserted between the Parylene surfaces and the glass slides to prevent Parylene sticking on the glass. External pressure is applied by stacking a ~ 2 lbs metal plate on top of a 75 × 50 mm glass slide, allowing Parylene to Parylene bonding at a low temperature. Then the whole unit is placed in the vacuum oven with a chamber pressure of ~10 Torr for heating. Nitrogen backfill is introduced to equalize heating temperature inside the chamber. The temperature ramps from room temperature to annealing temperature, and then soaks at the anneal temperature for 2 days, followed by slowly cooling to the room temperature. The bonding results under different annealing temperatures are evaluated by

visual inspection, showing that delamination happens in samples annealed at 200 ºC, while good bonding results can be obtained in samples annealed at temperature above 250 ºC (Figure 4.12).

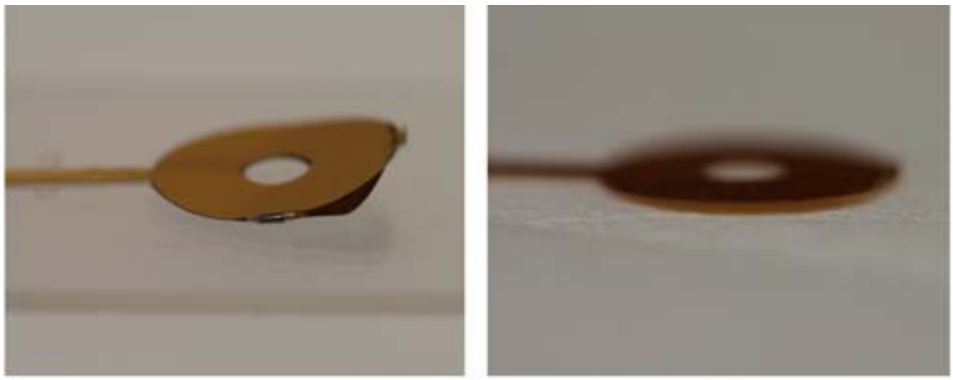


Figure 4.12: Thermal bonding results of: (a) Sample annealed at 200 ºC shows delamination; (b) Good sample annealed at 250 ºC.

It is also found that the samples remain flexible after bonding (Figure 4.13), indicating that annealing at temperature below melting point of Parylene C (290 ºC) will not affect its mechanical flexibility. The DC resistance of the samples is measured before and after bonding with no significant change observed, confirming the ductility and durability of metal traces. However, stretching marks and Parylene cracks are observed along the folding line after thermal treatment as shown in Figure 4.14, which is probably caused by stress concentration in the area of folding. Additional Parylene layer can be coated after thermal bonding to cover the cracked Parylene to ensure a good sealing for final devices.

Figure 4.13: Flexibility demonstration of the folded-and-bond devices.

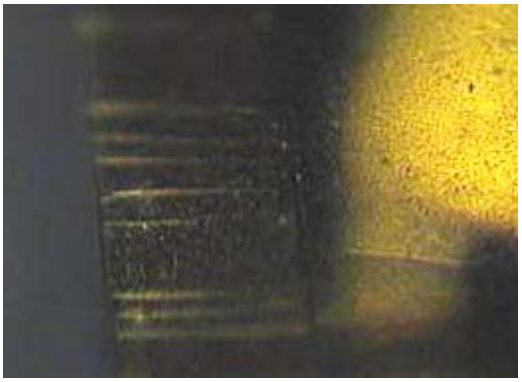


Figure 4.14: Stretching marks along the folding line.

4.3.3 **Fabrication and testing results**

Figure 4.15 (a) presents the final product of the Parylene-based coils as shown in Figure 4.11 (a) after folding and bonding. The thermal bonding process is performed in vacuum at 250 ºC for 2 days with weight compression. Different layers are hand aligned using an Olympus SZ-STB1 stereoscope with 4× magnification (Olympus American, Center Valley, PA), with alignment errors of 10 μm to 30 μm (Figure 4.15 (b)). These coil prototypes are specifically designed for intraocular retinal prosthesis with the design parameters described in Table 4.1. Another 5 μm of Parylene C is deposited to cover the entire devices except the pad areas, and therefore the total thickness of devices is approximately 25 μm.

(a) (b)

Figure 4.15: (a) Fold-and-bond coils after thermal bonding. (b) Overlapping metal wires with misalignments of 10 μm to 30 μm.

Table 4.1: Design specifications of the fold-and-bond coils.

Coil type	ID (mm)	OD (mm)	Number of turns	Number of layers	Width of wires (μm)	$R_s(\Omega)$	$L_s(\mu H)$	$C_s(pF)$	Q at 1MHz
I	3	10	28	2	220	29	5	65.5	1.1
II	3	10	48	2	120	90	14.8	64.5	1

The electrical characteristics of the fold-and-bond coils are analyzed using an Agilent 34401A multimeter and an HP 4192A LF impedance analyzer before and after thermal bonding. The lump parameters are extracted from the 3-element model and summarized in Table 4.2. As expected, the Q-factor of the coil is increased by more than 90% for both prototypes after folding. Changing the wire width does not have significantly influence on the parasitic capacitance, indicating the capacitance between adjacent layers is dominant over the capacitance between turns. Coil prototype I shows a higher ESR than the theoretical value (29 Ω), which may be caused by non-uniform metal thickness

produced by e-beam evaporation. Besides fabrication imperfections, misalignment between layers can also contribute to this deviation. Overall speaking, however, the measured values are in good agreement with the theory.

Table 4.2: Extracted electrical parameters of fold-and-bond coils.

Coil type		$R_s(\Omega)$	$L_s(\mu H)$	$C_s(pF)$	Calculated Q at 1MHz	Q-factor enhancement
I	Before bonding	41.2	2.9	---	0.44	
	After bonding	41.8	5.70	62.1	0.86	95%
II	Before bonding	91.3	8.5	---	0.58	
	After bonding	92.2	16.3	70.8	1.11	91%

The Q factors as a function of frequency are also measured, as shown in Figure 4.16. It can be seen that the Q factors follow the theoretical curves of $\frac{\omega L_s}{R_s}$ at low frequencies. As frequency increases, the measured curves reach maximum values at certain frequencies (f_m), and then drop to zero at the coil self-resonant frequencies due to parasitic capacitance. Correlated to the lower self-resonant frequency (f_r), the Q factor of the coil with higher inductance reaches the maximum at a lower frequency, which can be calculated as $\frac{f_r}{\sqrt{3}}$. In addition, it should be noted that, for coils with the same number of metal layers, their Q factors are almost identical at frequencies below f_m, confirming that inductance enhancement on single layer would not contribute to the total Q factor, as the coil ESR will be simultaneously increased by adding more wire turns. However, the

maximum quality factor of the coil decreases as the coil inductance increases (Figure 4.16), which is due to higher dissipated energy caused by larger coil resistance [84].

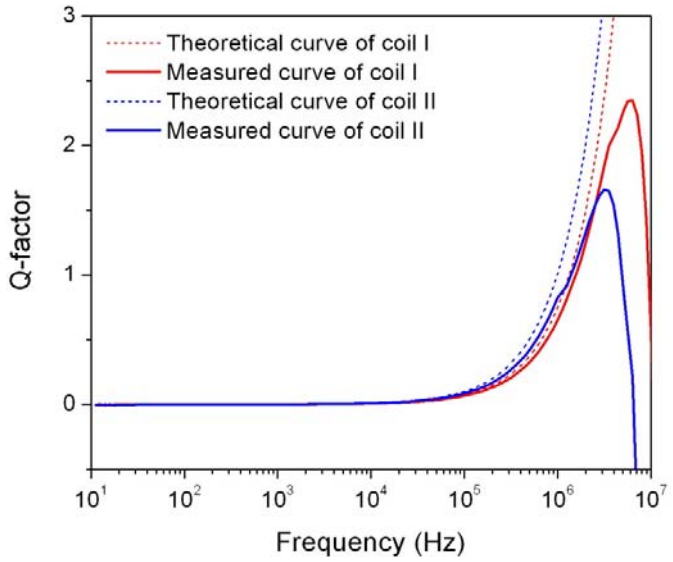


Figure 4.16: Q-factors as a function of frequencies.

The power transfer effect is tested using a simplified inductive link with a pair of coils, as shown in Figure 4.17. In this setup, the transmitter coil is hand-wound with a self-inductance of ~ 23 μH and a series resistance of ~ 1.5 Ω. The inner diameter of the primary coil is optimized to be ~30 mm, using Equation 3-26 in Section 3.4 . The receiver coil is the MEMS coil presented in Figure 4.15. The primary stage is driven by an HP E3630A function generator with a sinusoidal input signal of 20 V peak to peak. Both the primary and secondary circuits are subject to parallel resonance with the same resonance frequencies. To minimize environmental interferences, the coils are covered with aluminum foils as electromagnetic shielding.

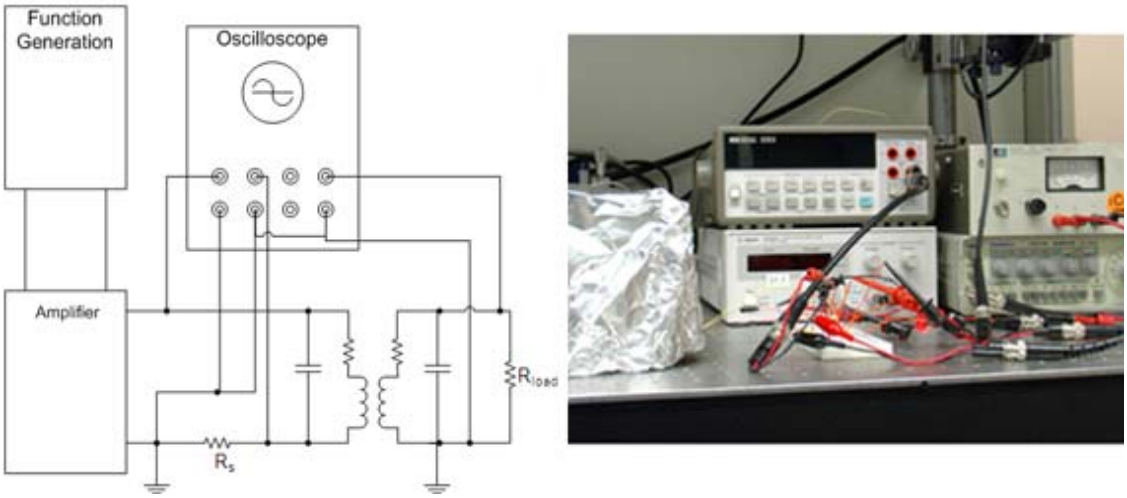


Figure 4.17: Experimental setup for power transmission measurement.

Preliminary experiments have been performed. To obtain the input power, a 10 Ω resistor (R_s) is incorporated in the primary stage to monitor the current. The voltage across the transmitter coil is then calculated by subtracting the R_s voltage from the output voltage of the amplifier. The transferred power, which is defined as the power delivered to a 1 kΩ load resistor (R_{load}), can be obtained by directly measuring the voltage across the load resistor. The power transfer efficiencies of two coil prototypes at 1 MHz are given in Figure 4.18, as functions of the separation distance between the coil pairs. The red curves show the experimental data and the black curves represent the theoretical prediction. It can be seen that the testing results match the theoretical calculation within a reasonable range. As expected, the coil prototype II, which has a higher Q factor, has higher power transfer efficiency at the same separation. Overall, the power transfer efficiencies are low and drop quickly as the separation distance increases. The power transfer efficiency is below 0.2% at the implanted depth of 15 mm, indicating more power will be required on the primary stage in order to obtain enough power for the implant components.

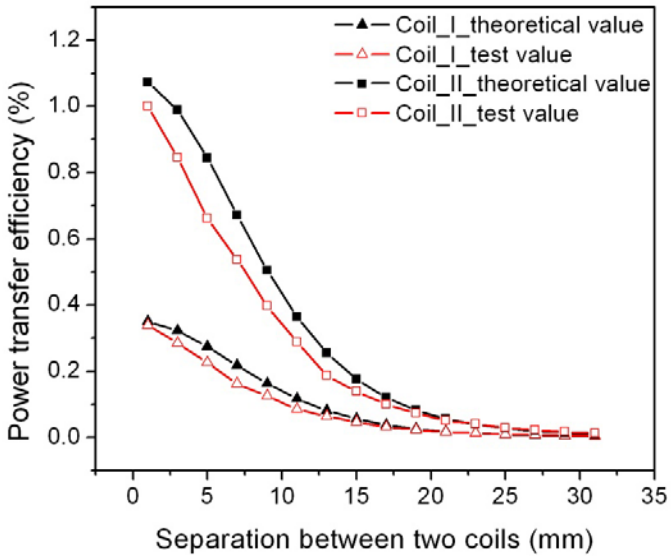


Figure 4.18: Power transfer efficiency at 1 MHz vs. separation distance of the coil pair.

The power transfer efficiency at different operation frequencies has also been measured, as plotted in Figure 4.19. The results show that the power transfer efficiency is enhanced by more than 3 times as the operation frequency is changed from ~1 MHz to ~2 MHz. This is because the effective Q factor increases by almost two times as frequency goes up (Figure 4.16). However, this Q factor is still far below the target number for our retinal implant system. Future direction for coil optimization will aim to increase the number of metal layers in order to improve the Q factor. According to the theoretical calculation, with a given gold thickness of ~ 2 μm, at least 20 layers of metal are necessary in order to achieve a coil Q factor of around 10.

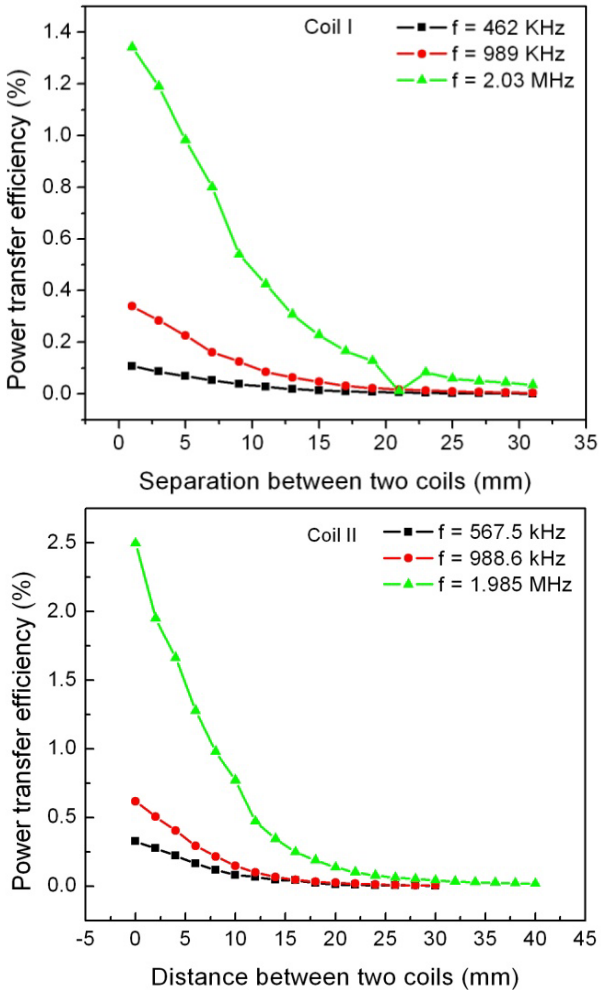


Figure 4.19: Power transfer efficiency vs. separation distance of the coil pair.

4.4 Summary

We have designed and successfully fabricated two types of MEMS coils using the Parylene-metal-Parylene skin technology. Experiments have been done to measure the electrical properties of the coils, which show good agreement with the theoretical values. The data transfer effect has been demonstrated at UCSC using the MEMS coil. However, the power transfer efficiency at a separation distance of 15 mm is below 0.5%, which is too low for high-density retinal stimulation. The most effective way to enhance the coil Q

factor is to increase the number of metal layers. While direct fabrication could be too complicated to carry out, the fold-and-bond technology has proven itself as a very promising alternative.

Chapter 5 IMPLANTABLE RF-COILED CHIP INTEGRATION TECHNOLOGY

5.1 Introduction

Despite successful device development, a significant hindrance to the future progress of the retinal project is system integration, which demands high lead-count interconnects and hermetic packaging without compromising flexibility and biocompatibility. Traditional packaging technologies which use wire-bonding, flip chip, and tape automated bonding do not meet these requirements due to their low reliability, non-biocompatibility, and high fabrication costs. A MicroFlex interconnection (MFI) technology has been developed [85], in which flexible polyimide substrates are fabricated as carriers, and individual devices are mounted to the polymer substrates using bump-bonding method. While devices packaged with this technology are flexible enough, their long term biocompatibility has not been fully proven. Its tedious and low yield process also makes it difficult and costly to integrate high electrode density devices.

To overcome the challenges encountered in these traditional technologies, a chip-level integrated interconnect (CL-I^2) packaging technology has been developed by Rodger et al. [86]. In this chapter, we will extend it to incorporate silicon housings and functional Parylene-based devices. The big advantage of this new technology is that it uses micro-electro-mechanical system (MEMS) techniques, enabling the integration of CMOS IC chips and prosthetic electrodes [4] to achieve high-level functionality. The chip-to-packaging interconnections are forged using standard microfabrication techniques including photolithography and metal etching; therefore, no wire-bonding, bump-bonding, or soldering are needed. Another advantage of our approach over traditional methods is

that the density of interconnections is limited only by photolithography resolution, which offers the possibility to achieve high-lead-count (> 1,000) integration. Finally, the favorable mechanical and chemical properties of Parylene C (Section 1.3.2) allow our final integrated system to be highly flexible and biocompatible for implantation.

5.2 Accelerated-lifetime soaking test of Parylene protected ICs

Before delving into the integration technology, it is important to study the Parylene sealing performance on IC circuitry. To do that, similar ALSTs are performed on Parylene-protected IC chips. An EM4100 read-only radio-frequency identity (RFID) chip (EM Microelectronic, Switzerland) is used as a sample chip. This chip is a CMOS integrated circuit with metal composition of Al-Ni-Au on contact pads. It can be powered up using an external coil with an electromagnetic field. By turning the modulation current on and off, the chip sends back a 64-bit sequence stored in the memory array. The operation frequency of the chip is between 100 kHz and 150 kHz, with 125 kHz being typical.

Unpowered soaking test is first performed in saline at 77 ºC. Samples are prepared by cleaning chips with isopropanol and DI water, followed by a Parylene C deposition of approximately 10 μm. Bare chips without Parylene coating are also tested as comparisons. During the soaking period, the samples are examined daily under a microscope. The test lasts up to six months, and then the samples are removed from hot saline for functionality measurement using a Wentworth Labs 11PO900 probe station (Wentworth Laboratories, Inc., Brookfield, CT, USA). As can be seen from Figure 5.1, the chip without Parylene coating experiences serious metal corrosion after only 2 days of soaking, while the samples

with Parylene protection has not observable metal damage even after six months of soaking. Functionality test is performed on the Parylene coated chip after removing the Parylene on contact pads with oxygen plasma etching or probe tip scratching. The result shows that the chip is still well functioning, indicating that IC circuits can remain intact in hot saline for six months with Parylene protection.

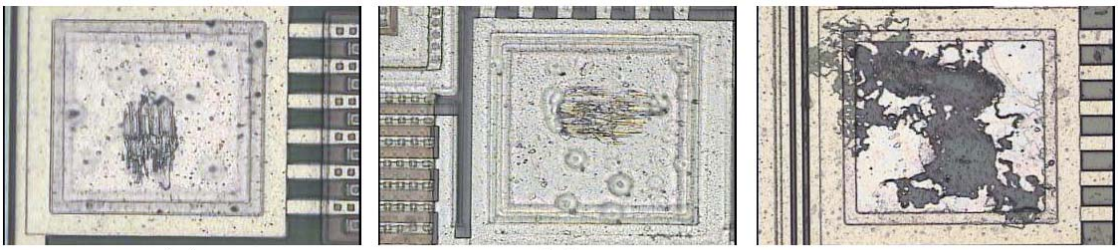


Figure 5.1: Microscope images of chip metal pads. (a) A chip coated with annealed Parylene C. (b) A chip with regular Parylene C after 6 months of soaking. (c) A bare chip after 2 days of soaking.

Given this exciting result, active soaking tests are conducted to further investigate the lifetime of the Parylene protected chip under continuous electrical stressing. In this case, the RFID chip is glued onto a Parylene cable using a biocompatible silver epoxy EPO-TEK H20E (Epoxy Technology, Billerica, MA, USA). The epoxy is fully cured and outgassed in a convection oven for 3 hours at 80 ºC. Regular wires are also pasted on the other side of the Parylene cable in order to connect the chip to external test units, as shown in Figure 5.2. The device is then conformally coated with Parylene C for testing.

The soaking test is performed in a convection oven. During the test, the device is held in a glass bottle filled with regular saline, and the wires are connected to an external coil. The external hand-wound coil has an inductance of ~5.3 mH and an ESR of 88 Ω at 125 kHz. A commercially available RFID reader module (Parallax Inc. Rocklin, CA USA)

is used to continuously send power and requests (24 hours a day) to the RFID chip though inductive coupling. The reader module contains an integrated coil with dimensions of 60 mm by 66mm, and is driven by a 5 volt DC supply. The output port of the reader is connected to an HP 54503A oscilloscope and a webcam is used to monitor the signal readout by taking a picture every 10 minutes (Figure 5.3).

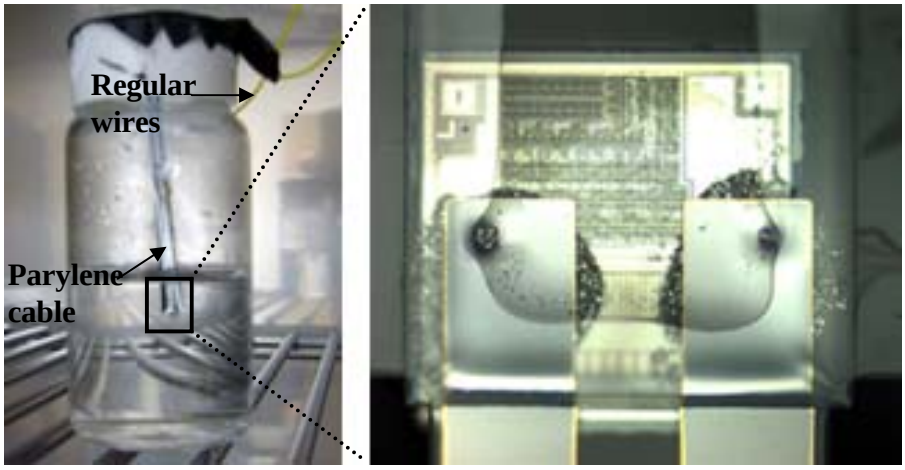


Figure 5.2: (*left*) Assembled RFID chip soaked in saline. (*right*) Close-up image of the attached RFID chip.

Figure 5.3: Test setup for the active soaking test of RFID chips.

Samples coated with different thicknesses of Parylene are tested at various temperatures. MTTF is defined as the time point when no output signal can be detected. Four samples are tested under each condition, and their MTTF and the standard deviation is plotted in Figure 5.4. According to the Arrhenius relationship, chips with 22.1 μm Parylene coating will have an MTTF of ~ 2 years at 37°C under the active condition. Ideally, samples with thicker Parylene coating should have better durability if failure is solely caused by water permeation through Parylene. However, the results show that samples with 22.1 μm Parylene coating do not show much advantage, indicating that other failure mechanisms besides water permeation might have taken place.

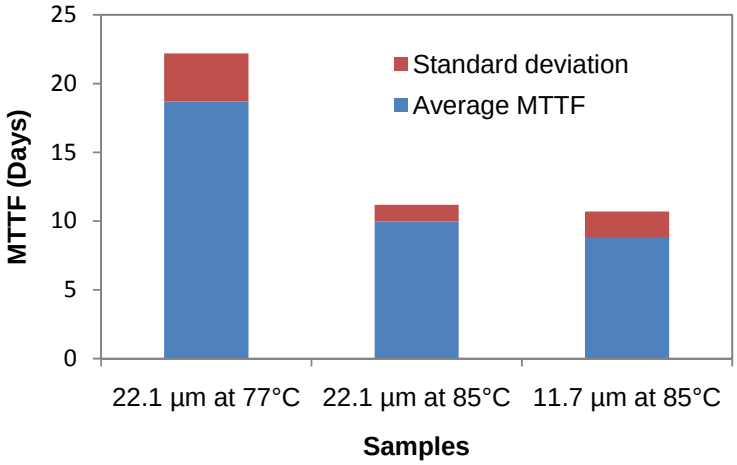


Figure 5.4: Active soaking test results of Parylene protected IC chips.

To find out the exact failure mode, the failed samples are examined using SEM. Parylene cracks are observed in samples with both 22.1 μm and 11.7 μm Parylene C coatings. The mechanism of Parylene cracking has not been fully understood. It is possible that the chip generates a lot of heat under intensive electrical stress so that thermal stress concentrates along the edges due to poor heat dissipation. Also, it is noted that the

test temperatures are very close to or within the range of the glass transition temperature of Parylene C (80 °C – 100 °C), therefore Parylene might undergo material property changes due to the recrystallization of the polymer chains. The active soaking test is still ongoing, and more experimental results are expected to enable a complete understanding of Parylene packaging behaviors.

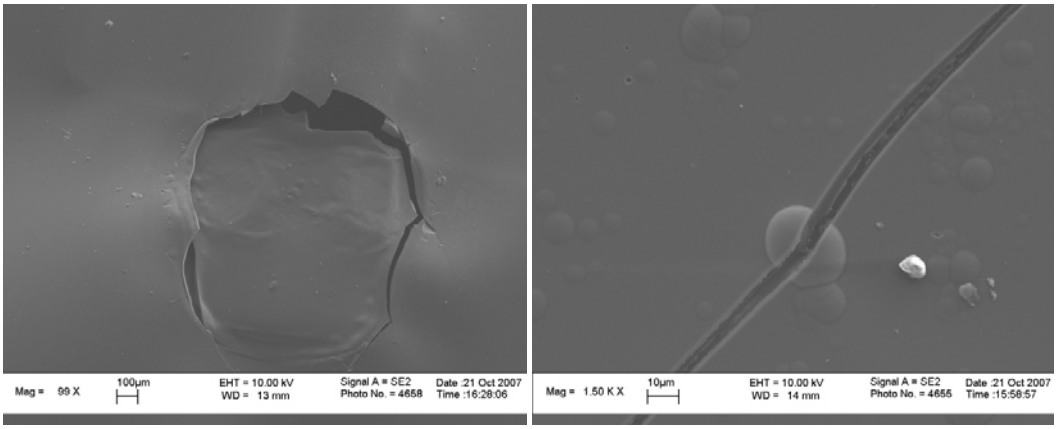


Figure 5.5: Parylene cracks is sample with (*left*) 11.7 μm Parylene coating and (*right*) 22.1 μm Parylene coating.

5.3 Integration demonstration

5.3.1 **Design and fabrication**

Figure 5.6 depicts a conceptual schematic of an embedded chip integration, in which individual prefabricated chips and passive components can be embedded in a carrier silicon wafer and sealed with Parylene C. After that, the fabrication of other surface MEMS components, such as electrode arrays and coils, can be performed on the same platform. To demonstrate this technology, the same EM4100 read-only RFID chip is used again as shown in Figure 5.7 (a). In order to determine the chip housing dimensions, the chip is imaged with a WYKO interferometer (Veeco Instrument Inc., Woodbury, NY,

USA), and is measured to have average dimensions of 1 mm in length, 0.98 mm in width, and 182 μm in thickness (Figure 5.7 (*right*)). A square planar coil is designed for wireless power and data transmission, which consists of two metal layers with 22 turns on each layer. The overall coil size is 2 cm by 2 cm. During the fabrication, the two coil terminals are connected to Pad_1 and Pad_2 on the chip (Figure 5.7 (*left*)). Due to the low power consumption of the wireless chip, only the coil is needed to power the circuit, and no extra capacitor is required.

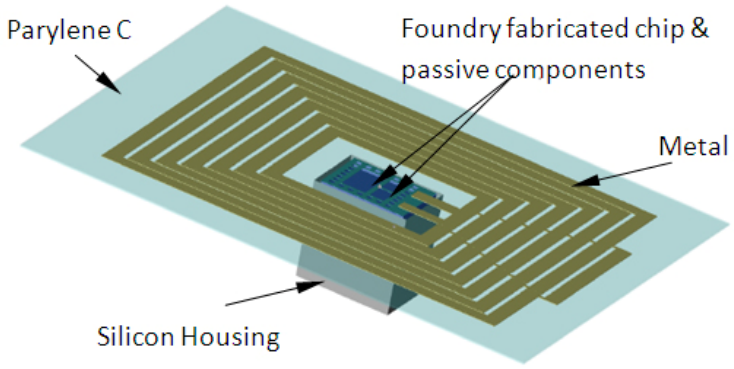


Figure 5.6: Concept of embedded chip integration.

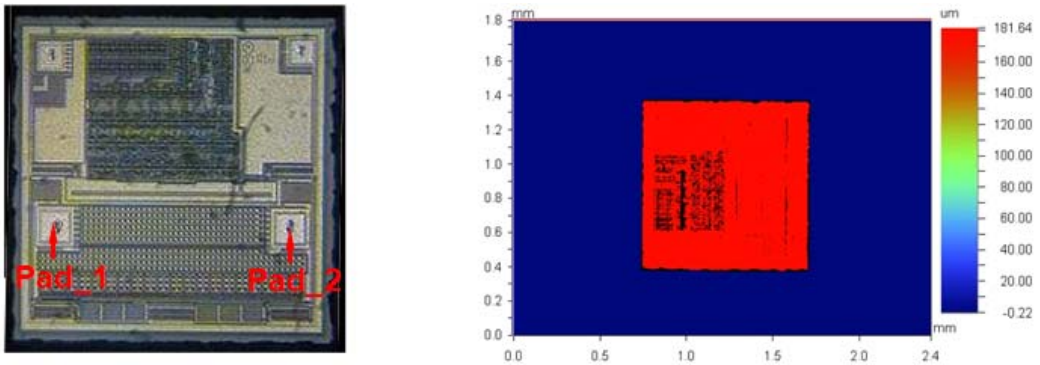


Figure 5.7: (*left*) EM 4100 RFID chip used to demonstrate the integration technology. (*right*) WYKO image of a typical chip.

Figure 5.8 illustrates the detailed fabrication process, starting with a standard 4 inch wafer that is ~550 μm thick and coated with a layer of sacrificial photoresist. A 5 μm layer

of Parylene C is deposited on top of the photoresist. To secure Parylene on the substrate, Parylene anchors surrounding the chip housings are etched into the substrate using Bosch process in a DRIE system (Unaxis Corporation, St. Petersburg, FL, USA) [87]. After Parylene deposition, a 500 nm layer of gold is deposited using an E-beam evaporator, and patterned to form the first layer of coil wires. Next, cavities matching the chip dimensions are etched into the Parylene and silicon using RIE and Bosch process, and the chips are then dropped into the cavities to self-align with an average lateral displacement of less than 10 μm. During this procedure, epoxy is applied to the bottom of the cavities as needed in order to compensate for cavity depth inaccuracy and to fill the gaps surrounding the chips. A metal pole with a flat silicon piece attached on one end is used to push the chips into the cavities and to level the surface (Figure 5.9). After the chips are fitted into the cavities, Parylene deposition is performed again to seal the chips and to form an insulation layer between two metal layers, followed by oxygen plasma etching to properly open interconnection vias. A second 500 nm layer of gold is then deposited and patterned to form the top layer of coil wires and interconnects. Another 5 μm layer of Parylene C is coated on top and patterned using oxygen plasma to define the profile of devices. Through-wafer trenches surrounding the chips are then etched from the backside using the Bosch process, and the Parylene-based coil is released from the substrate, carrying the chips encapsulated in silicon housings. Lastly, the entire device can be sealed with Parylene for protection.

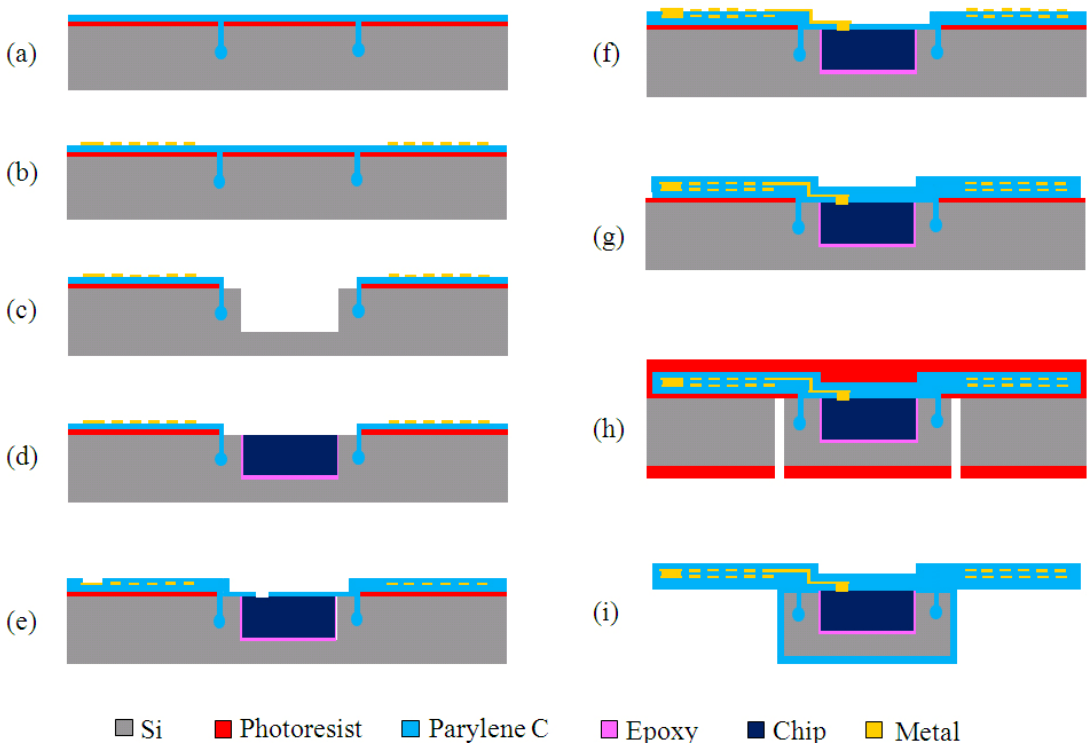


Figure 5.8: Detailed process flow for embedded chip integration.

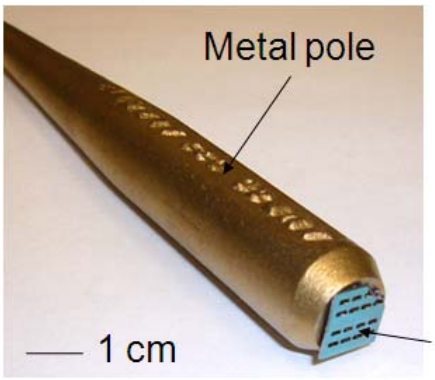


Figure 5.9: Metal pole with a silicon piece for use to push the chip to the silicon shell.

In this integration technology, minimizing the vertical displacement of the chip from the wafer surface is crucial for subsequent photolithography and metallization steps. Large vertical displacements will result in broken wires around the chip. To better control the process, the surface heights of the chips are measured using a stylus profilometer P-15 (KLA-Tencor, San Jose, CA, USA) after the chips anchor in place in the silicon shell.

Figure 5.10 shows the surface profiles of four successfully integrated chips with respect to the surrounding wafer. The overall vertical displacements from the wafer surface are within 6 μm, providing sufficient flatness for further processes.

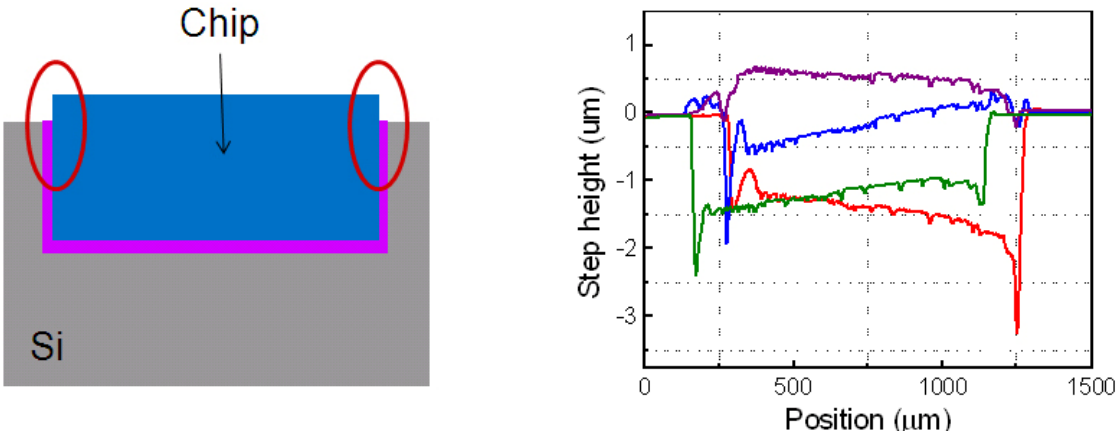


Figure 5.10: Vertical displacements of chips: 0μm step height indicates wafer level.

Another important aspect is the horizontal alignment of perimeter interconnects to the embedded chips, which limits the interconnection density of the integration. By design, the chip should be self-aligned in the silicon shell within 10 μm of lateral displacement; however some chips are misaligned by more than 10 μm due to the dimension variation of the chips themselves (Figure 5.11). With tighter tolerance on cavity sidewalls, or with more precise chip-alignment lithography, this alignment deviation can be reduced in the future to achieve high-lead-count integration.

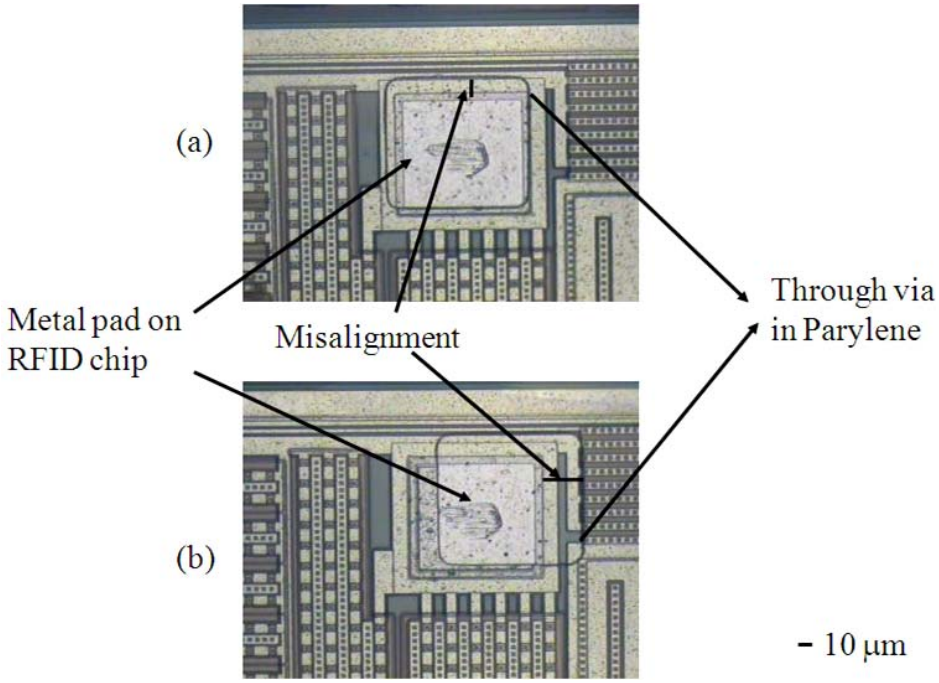


Figure 5.11: (a) Example of <10 μm lateral misalignment of the chip; (b) Example of >10 μm lateral misalignment of the chip.

5.3.2 **Fabrication and functional test results**

We have successfully integrated the RFID chip with the Parylene-based RF coil, and Figure 5.12 (a) shows an example of fabricated devices. In this device, the self-inductance of the receiver coil is around 16 μH measured with an HP 4192 impedance analyzer, and the DC resistance is around 275 Ω measured with an Agilent 34401 multimeter. The total thickness of the Parylene-metal-Parylene thin film is approximately 20 μm. Thank to the flexibility of Parylene, this final device is very flexible, allowing the device to be placed in direct contact with delicate tissues during surgical implantation (Figure 5.13).

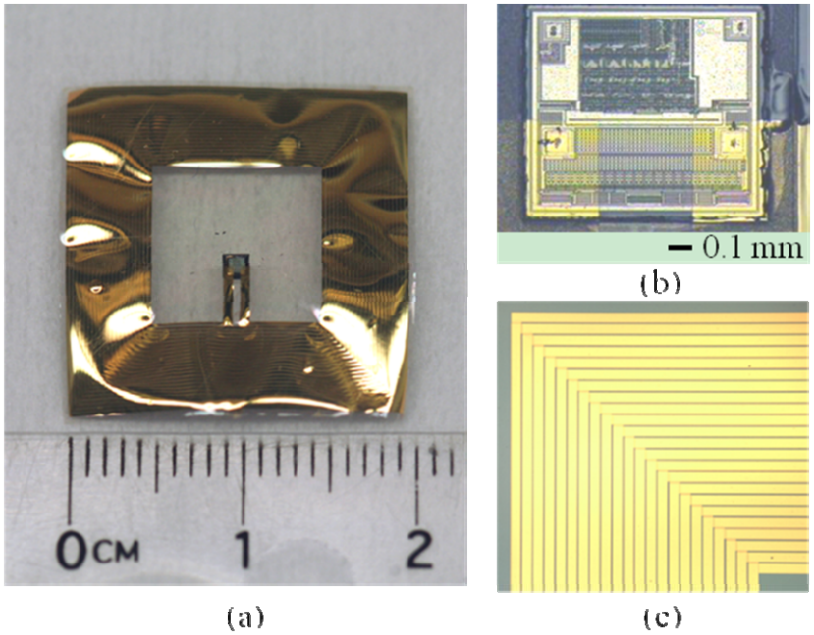


Figure 5.12: A fabricated device: (a) Overall view of the device. (b) Close-up view of the embedded chip. (c) Close-up view of the coil wires.

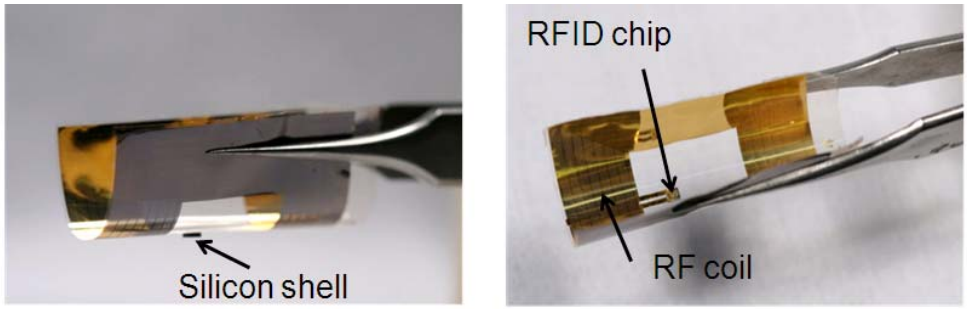


Figure 5.13: Flexibility of the Parylene-metal-Parylene thin film.

The functionality of the embedded RFID chip is tested with the Parallax RFID reader module, as shown in Figure 5.14. The output port of the reader is connected to an oscilloscope to monitor the signal readout. When the coil-integrated RFID is placed within reading distance of the reader, the information stored in the chip will be detected by the reader, and an 8-bit transistor-transistor logic (TTL) signal sequence can be observed on the oscilloscope, as shown in Figure 5.15. The spatial separation between the primary coil and secondary coil is varied during measurement, and a maximal detectable range of 3 mm to 4

mm is found. This short reading distance is mainly due to the low Q-factor of the receiver coil which is calculated to be approximately 0.05 at 125 kHz, and therefore results in low power transfer efficiency through the electromagnetic field.

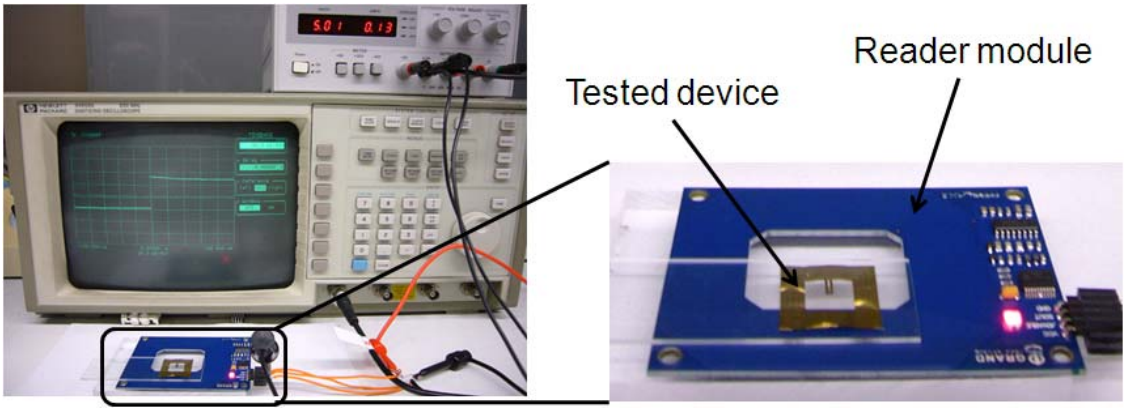


Figure 5.14: Test setup to verify the function of embedded RFID chips.

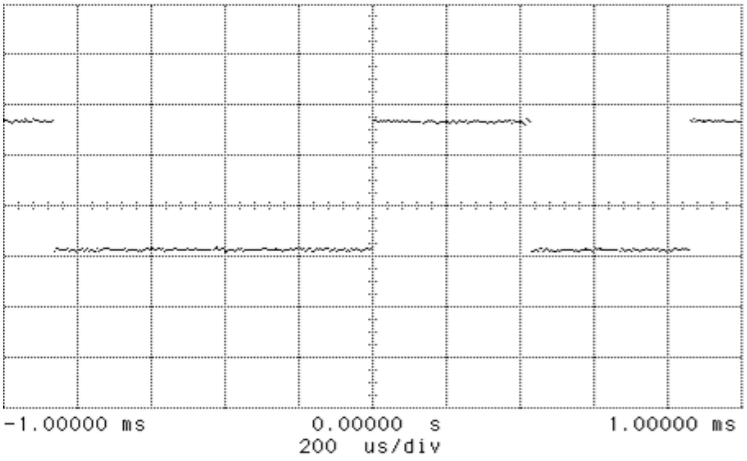


Figure 5.15: Signal readout from the oscilloscope.

5.4 Mechanical model for implantation studies

We have developed and demonstrated an integration technology to incorporate a prefabricated chip in a Parylene-based system. Naturally, the next step is to build a monolithic intraocular system using this integration technology, followed by the

demonstration of *in vivo* retinal stimulation using such a system. However, due to the small volume and complex anatomy of human eye, it is important to carefully evaluate possible system geometries prior to finalizing the specifications. In addition, it is necessary to study the feasibility of surgical implantation in animal models to determine optimal implantation techniques, and to verify the robustness of the devices and materials under surgical manipulation. Therefore, an intraocular test system is designed (Figure 5.16) and fabricated in Parylene C using a photoresist mask and oxygen plasma etching, simulating the mechanical integration of various key components using size-matching dummies. The design includes an RF coil, intended to be implanted in front of the iris. A flexible cable is passed through the anterior and posterior lens capsule into the vitreous cavity, and an electrode array with a 450 μm diameter tack hole is attached to the retina using a retinal tack. In order to reduce fabrication complexity, the coil part and the array part are separately fabricated in this dummy system. The coil cable is heat-molded to form a "U-shape" curvature after fabrication, rounding the anterior and posterior capsulotomies into the vitreous cavity during implantation. Dummy coils, which have the same dimensions as final devices, are then glued onto the coil part using biocompatible epoxy EPO-TEK 301-2. Similarly, the array part is heat shaped using a custom 6061 aluminum mold comprising a recessed concave region and a mating stainless steel sphere that approximates the curvature of the canine retina (diameter ~22 mm), as shown in Figure 5.17. During annealing, the array part is sandwiched between the sphere and the mating surface, while the cable is pressed flat against the aluminum surface. After that, dummy chips are glued onto the Parylene cables in one of the possible positions anticipated for the ASICs. Finally, the two

separate parts (the coil region and the array region) are bonded together using epoxy. The curing condition for this particular epoxy is 80 °C for 3 hours in a convection oven.

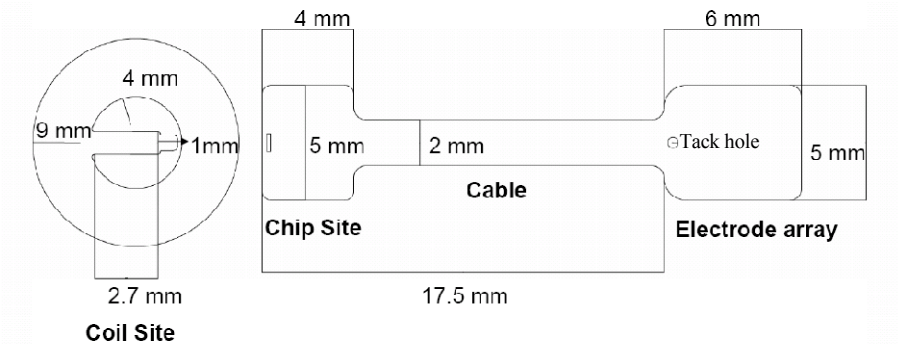


Figure 5.16: Prototype geometry for an all-intraocular Parylene-based device with all required component regions for a completely implantable system.

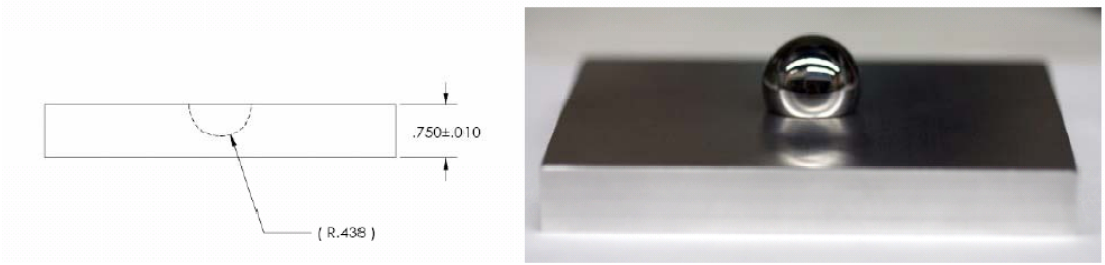


Figure 5.17: Custom heat-forming mold. (Images courtesy of Dr. Damien Rodger)

Two prototypes for acute implantations are designed and fabricated (Figure 5.18), showing an overall Parylene thickness of approximately 18 μm. For the model designed for test chip integration, the coil is made from aluminum foils with dimensions of ~3.75 mm in inner diameter, ~9 mm in outer diameter, and ~200 μm in metal thickness. The test chip used in this model is a BION stimulator designed for neuromuscular prostheses [88]. As for the IRP model, the coil and the chip model are both made of acrylonitrile/butadiene/styrene (ABS, RedEyeRPM, Eden Prairie, MN, USA). The coil has dimensions of ~7 mm in inner diameter, ~11 mm in outer diameter, and ~1.5 mm in thickness. The chip model is a hexahedron with dimensions of 6 mm × 6 mm × 2 mm. In

the final system, this part is actually a hexahedral can which has all electronic components integrated and packaged in it.

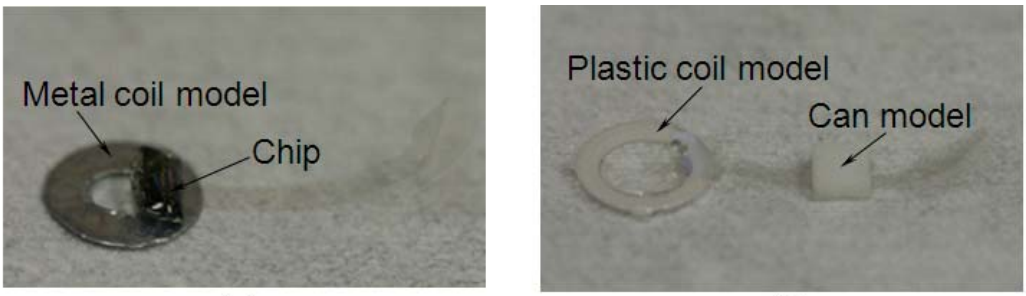


Figure 5.18: Two surgical models for acute implantation: model-I (a) is designed for test chip integration; model-II (b) is designed for IRP1K integration.

These test models are then implanted in a canine eye to evaluate surgical approaches and to determine the system geometrical feasibility inside the eye. Example surgical photographs are given in Figure 5.19. A significant problem with these initial designs is that the chip positions are not optimal, which induces surgical difficulties. For instance, the chip is too close to the coil site in the test chip surgical model, blocking the view during implantation so that it is difficult to see the tack hole on the array site. In the IRP surgical model, the dummy chip is attached partway down the Parylene cable, therefore the view is less obstructed. However, we still have trouble with locating the tack hole because the chip module is near the array part and blocks the view of the surgeon during the operation. In addition, the coils are floating in the anterior chamber in both cases, but they do need to be anchored into the angle to achieve excellent alignment and coupling. Finally, the cable length is too short for this canine eye, which tends to draw the coil against the iris during array tacking. This could become a serious problem if the pulling force was too big, which would damage delicate tissue in eye.

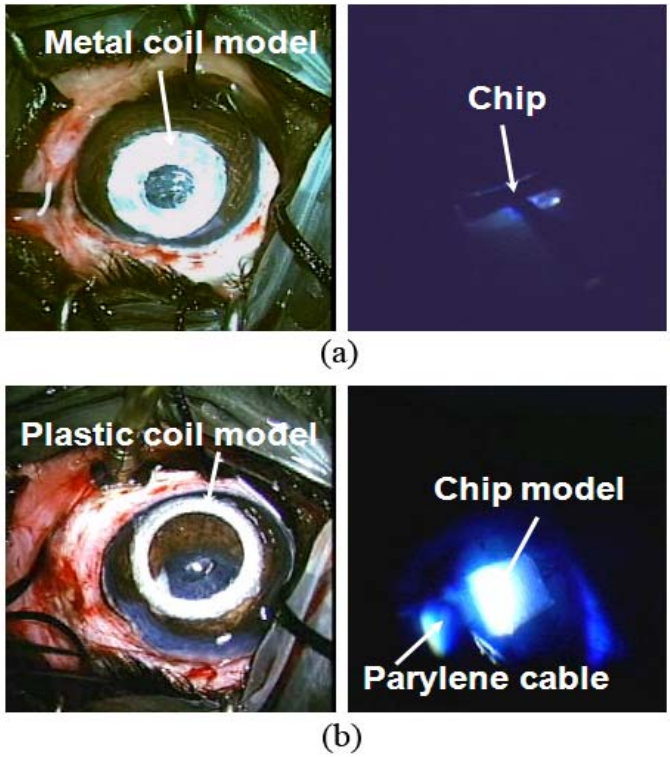


Figure 5.19: Example surgical photographs of prototype geometry implantation using (a) test chip surgical model; and (b) IRP1K surgical model.

To address the surgical problems encountered by the first batch of prototypes, an improved model is designed (Figure 5.20) in which the chip part is moved further away from the coil part, towards the middle part of the Parylene cable. The chip is attached along the cable rather than perpendicular to the cable. The inner diameter of the coil is increased to 5 mm, allowing a clearer view of the fundus during and after the surgery. To anchor the coil to the angle of the anterior chamber, a commercially available anterior chamber intraocular lens (ACIOL) (Model # 122UV, Bausch & Lomb, Rochester, NY, USA) is half-cut, and the haptics are attached to the coil, as show in Figure 5.21. After all components are glued together, a 1 μm layer of Parylene is deposited everywhere to

improve the biocompatibility of final devices. Two cable lengths are investigated for canine eyes, while the precise dimensions will vary for human implantations.

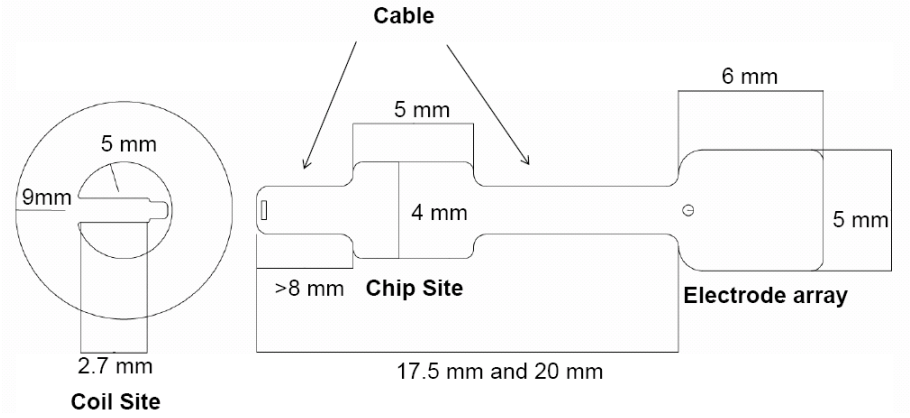


Figure 5.20: Improved geometry for a completely implantable system.

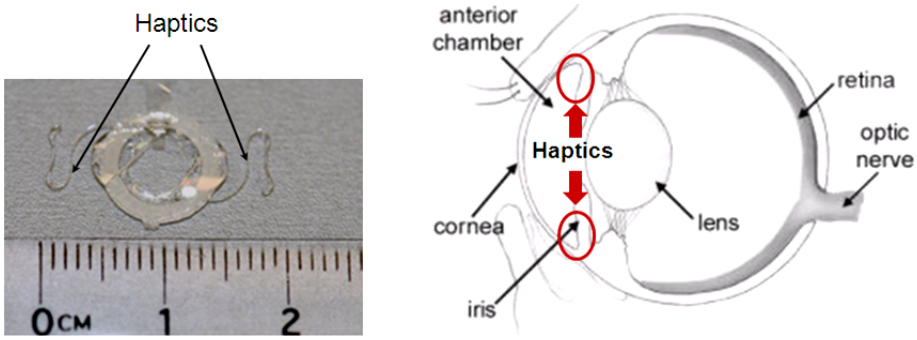


Figure 5.21: Example of a coil with ACIOL haptics attached.

The proposed devices are fabricated (Figure 5.22), and tested for *in vivo* implantation is operated at the Keck School of Medicine of USC. First, an incision approximately 10 to 11 mm long is cut in the cornea, followed by an anterior capsulorhexis. The lens is then extracted using phacoemulsification. After that, a posterior capsulotomy is made, and the vitreous is removed from the posterior chamber. The chip and array parts are then inserted into the posterior chamber through both holes in the lens capsule, leaving the coil part anchored in front of the iris. Vitrectomy is performed through the sclera ports, and the array part is tacked in place on the retina. Finally, the cornea and

the sclera ports are sutured closed, and the dogs are kept alive with devices implanted to evaluate the mechanical and biocompatible stability of the devices inside the eyes. Figure 5.23 gives examples of intraoperative surgical photographs.

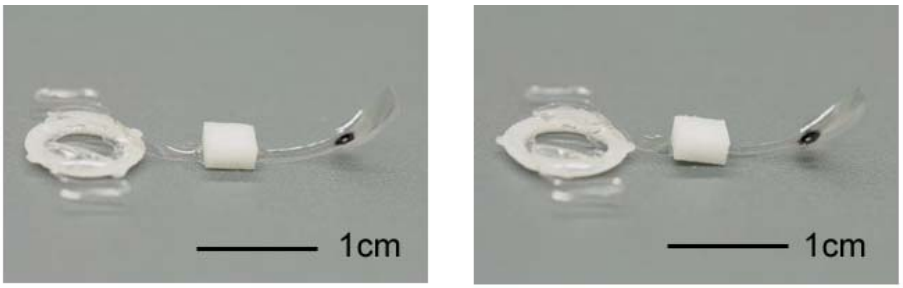


Figure 5.22: Two surgical models for chronic implantation in canine eyes.

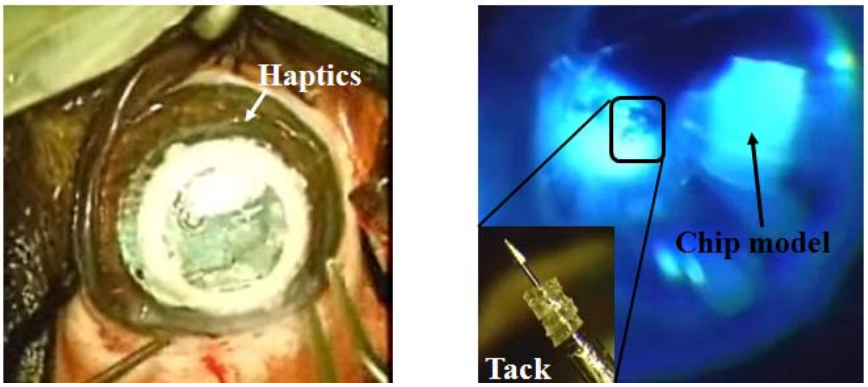


Figure 5.23: Surgical implantation photographs of improved surgical model under: (*left*) anterior illumination, and (*right*) intravitreal illumination.

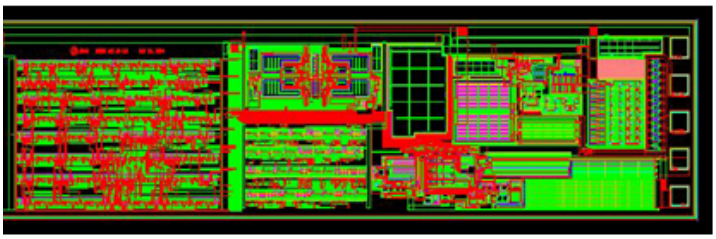
The surgical implantation indicates that the modified design results in a better surgical outcome, and that the haptics significantly help the coil region to anchor within the angles. However, serious inflammation is observed in both eyes a week after implantation, which is probably caused by toxins released from the epoxy. To further address this matter, the epoxy needs to fully cure and outgas before implantation. A thicker Parylene coating on the epoxy will also improve the isolation of the epoxy from eye environment.

5.5 Test chip system integration

5.5.1 Functional system prototype

A completely integrated system is designed according to the preliminary results of the surgical implantation of the mechanical models, employing the BION chip as a test chip. The BION chip is a single-channel stimulator chip which is initially developed to mimic muscle spindle function, and to help patients who are suffering from muscle paralysis. Once implanted into paralyzed muscles, the chip can receive both power and command signals through inductive coupling over a 480 kHz~500 kHz power carrier generated in an external unit, allowing them to emit precisely timed stimulation pulses with a highly regulated amplitude and pulse-width [88]. There are several reasons to select the BION chip as the test chip. First of all, chips specifically designed for retinal implantation are currently unavailable. The BION chip therefore becomes a reasonable substitute since a BIONic system includes all major components required for a final retinal implantation system. In addition, the BION chip consumes less power compared with the circuitry used in retinal implantation so that our current coil prototype might be able to deliver sufficient power for the chip operation. Finally, its integration process will involve the same embedded chip technique which can be easily repeated for retinal implantation.

Figure 5.24 shows the layout of the BION chip, and the pad functionalities are described in the right table. This chip has small physical dimensions of ~1 mm in width, ~2.33 mm in length, and ~257 μm in thickness. There are five pads on the chip with dimensions of approximately 120 μm × 74 μm. The distance between adjacent pads is approximately 110 μm.



Name	*Functionality*
V++	Rectifier output
A Coil	Coil terminal
B Coil	Coil terminal
Ta	Stimulation output
Ir	Common ground

Figure 5.24: BION chip layout and the pad connection.

The integrated system consists of a BION1-3 CMOS chip, two capacitors, a specially designed MEMS coil for RF power and data transmission from an external personal trainer, as well as a carrier substrate with a 2-electrode array, interconnection leads, and contact pads for system assembly. Physical dimensions of the devices are to meet the specifications predetermined by previous surgical implantation results. Figure 5.25 shows a system schematic and its corresponding circuit connections, where the on-chip rectifier is represented using a full-wave rectifier. C_2 is an off-chip charge storage capacitor which has a capacitance of ~22 nF, provided by Loeb's group. C_1 is a tuning capacitor in parallel with the receiving coil in order to achieve a resonant frequency of approximately 480 kHz. C_3 is used to simulate the tissue capacitance between the ground electrode and simulation electrode, which varies in different implantation environments, and thus is not included in our integration system. Ceramic chip capacitors (AVX Corporation, Myrtle Beach, SC, USA) are selected because they are about 1 mm × 0.5 mm × 0.56 mm in size and can be embedded in a standard silicon substrate.

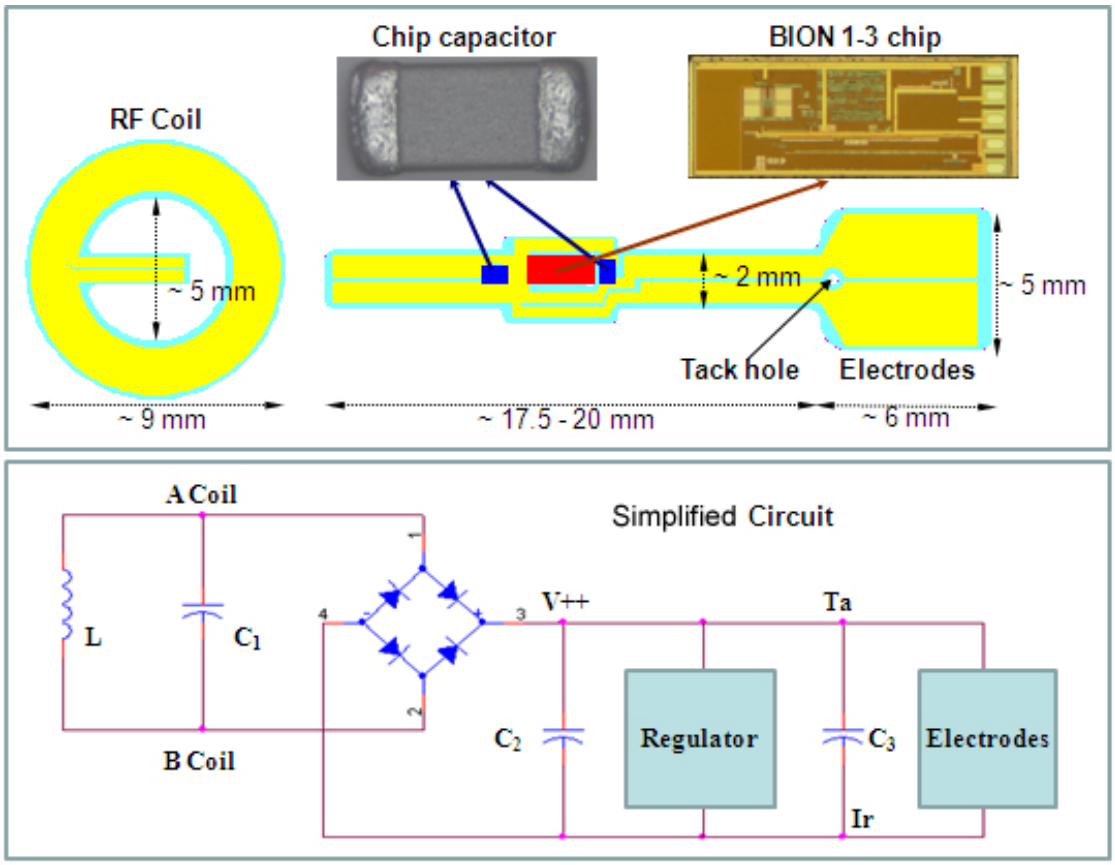


Figure 5.25: Schematic overview of a BION chip integration system.

5.5.2 **Fabrication of the assembled BION system**

Before building a monolithic system with the complicated CL-I^2 integration technology described earlier, it is important to calibrate each individual component, as well as to verify the system functionality. Therefore, it is worthwhile to make an assembled system by interconnecting components together on a Parylene substrate with conductive silver paste. The fabrication is divided into three steps: carrier substrate fabrication, RF MEMS coil fabrication, final system assembly and packaging. Figure 5.26 depicts the detailed process for making the carrier substrate. Parylene-C is first deposited on a silicon substrate. Then a 200 nm layer of metal is E-beam evaporated on the Parylene, and

patterned using lift-off to form connection pads, interconnection leads, and electrode sites [35]. Platinum is selected as the electrode material for optimal simulation capability, and no adhesion metal layer is needed in this case because platinum and Parylene are known to have good adhesion. After metal lift-off, another layer of Parylene is coated to seal the entire structure, followed by oxygen plasma etching in an RIE machine with a photoresist mask to define the outer geometry of the substrate, as well as to open the electrode sites and the contact vias. Finally, the device is peeled off from the silicon substrate in a water bath.

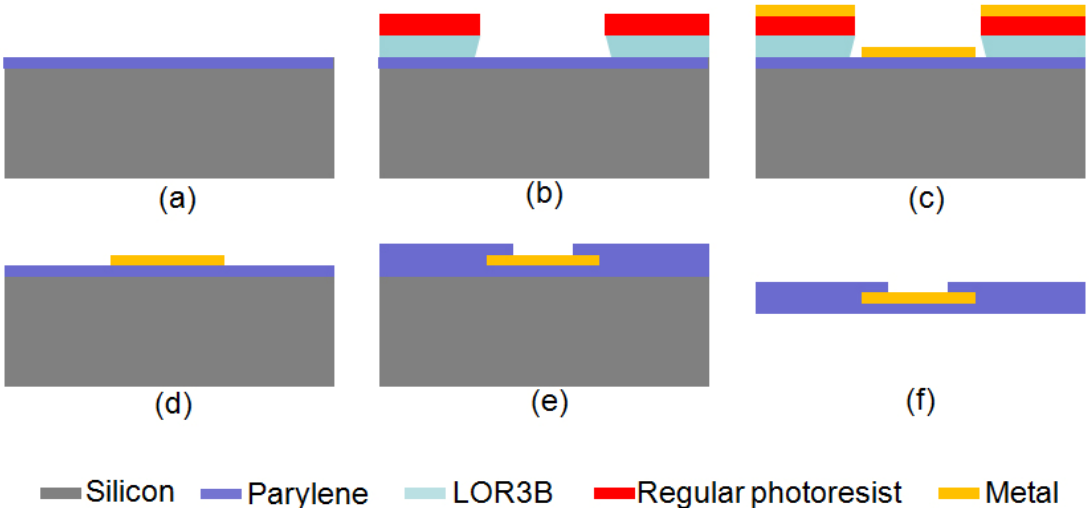


Figure 5.26: Fabrication process for the Parylene-based carrier substrate. Steps (b)-(d) describe the lift-off technology for platinum patterning.

Figure 5.27 presents a fabricated device, and the microscope image shows a special chip site design, where Parylene ribbons are etched in a way such that the chip can be held in place and aligned to the contact vias on the carrier substrate during assembly.

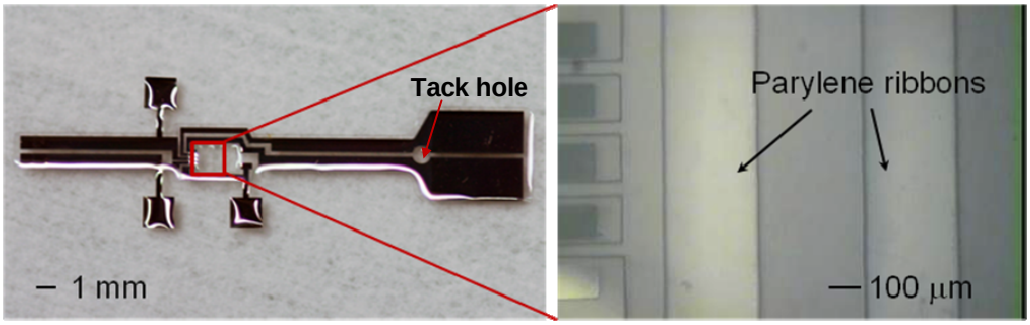
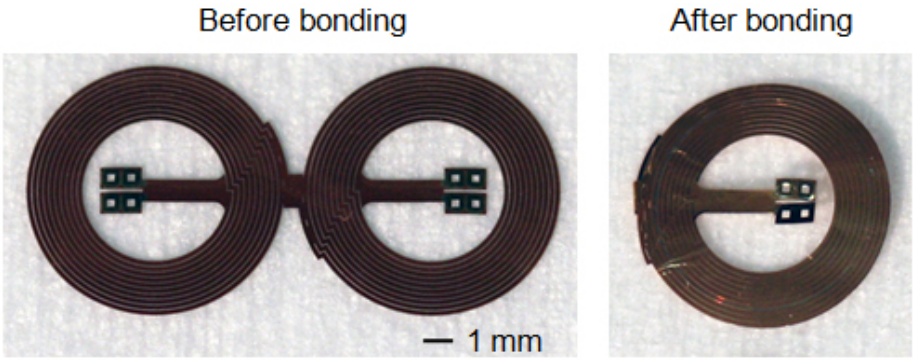


Figure 5.27: (*left*) Fabricated carrier substrate. (*right*) Parylene ribbons to hold the chip.



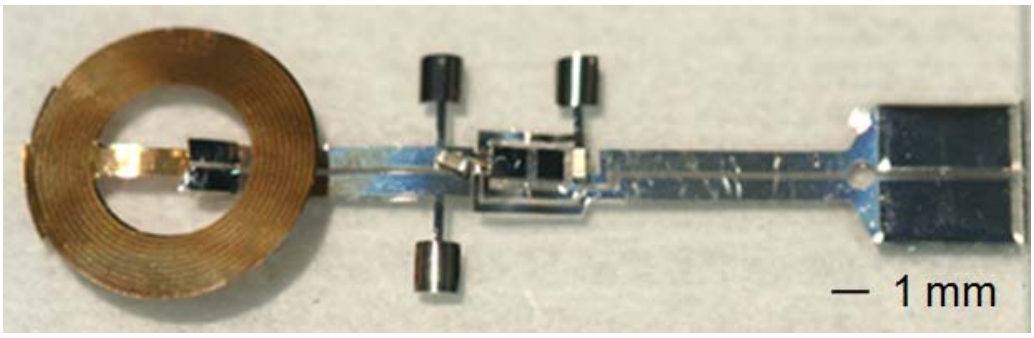
Inductance	DC resistance	Q at 500kHz
2.24 μH	15.82 Ω	0.45

Figure 5.28: A fabricated fold-and-bond coil with two layers of metal. The electrical characteristics are measured and given in the table.

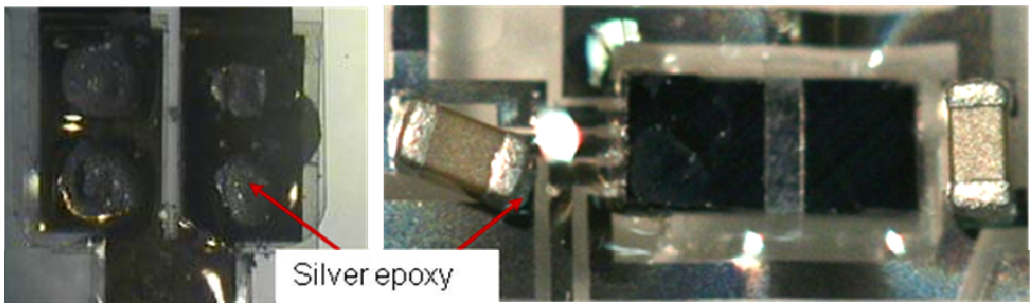
To fabricate the MEMS coil, the fold-and-bond technology is involved as discussed in Section 4.3.2 . Two single coils are placed in series, and made of a 3 μm layer of gold to achieve low resistance and high Q-factor. Then the device is folded into two layers and bonded together thermally. A fabricated fold-and-bond coil is shown in Figure 5.28, comprising two layers of metal with 10 turns in each layer. In-and-out leads are connected to the carrier substrate from the center, facilitating the surgical procedure. Through vias are designed to overlap with the contact pads, so the interconnections to the carrier substrate can be formed from both sides. Coil electrical properties are measured, showing an

inductance of ~ 2.24 μH and a DC resistance of ~ 15.82 Ω, which gives a Q factor of 0.45 at 500 kHz.

For hybrid system assembly, individual components (the BION chip, the coil and the capacitors) are aligned to the corresponding interconnection vias on the carrier substrate. A small amount of biocompatible silver epoxy (EPO-TEK H20E) is then applied on the contacts and cured at 80 ºC for 3 hours. The conductive epoxy serves two purposes: to form the interconnections between the components as well as to bond the components onto the carrier substrate. Figure 5.29 shows an assembled BION system, and close-up views on the interconnections for each individual component.



(a)



(b)

Figure 5.29: (a) A assembled BION system. (b) Interconnects formed with biocompatible conductive silver epoxy: (*left*) coil contacts, (*right*) chip and capacitor contacts.

Although this epoxy interconnection method is quick and easy, a main problem encountered during the fabrication is the lack of control of the epoxy amount when applied by hand (Figure 5.30). Short circuits can be created if too much epoxy is applied. Epoxy reflow can also happen during high temperature curing, resulting in short circuits. For chips with high density pad layouts, hand assembly is no longer applicable, and thus wafer level integration technology is necessary.

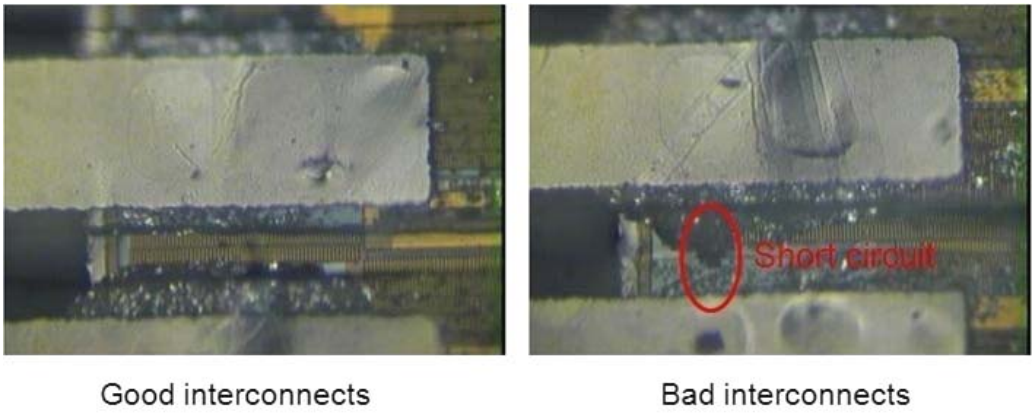


Figure 5.30: Examples of chip interconnections. For the right sample, short circuit is formed between adjacent pads.

Another big concern for this assembly technology is the isolation of the silver epoxy from the eye environment. It is well known that human eye is a delicate and sensitive organ, and any toxin released from the epoxy can cause inflammation and infection. In addition, eye fluids are very corrosive to exposed metal, which can reduce the durability of silver epoxy bonding, and finally result in open circuits. In order to overcome these problems, a layer of Parylene is coated to seal the entire system after assembly, just leaving the electrode site open.

5.5.3 **Functional test of the assembled BION system**

After the assembled system is made, its functionality is verified using a telemetry setup, as shown in Figure 5.31. The primary stage, which comprises a personal trainer unit, a class-E coil driver and a hand-wound transmitting coil, can generate a power carrier of ~500 kHz. The personal trainer stores command programs personalized for individual subjects, records the time and duration of treatment, and transfers this information to a computer for real time monitoring. Up to three programs can be loaded into the memory of the personal trainer [89]. The coil driver is connected to the personal trainer through a custom made adapter. The transmitting coil has an inductance of ~ 46.4 μH and a Q factor of ~118 at 500 kHz. Litz wires 1025-44 SPN are used for winding the primary coil in order to reduce the skin effect and proximity effect losses, where 1025 represents the number of strand in each bundle, and 44 represents American wire gauge per strand which is 50.8 μm by definition. The transmitting coil is built in a solenoid shape to establish a more uniform electromagnetic field inside the coil. Additionally, ferrite cores are incorporated in the transmitting coil to magnify the electromagnetic field and to improve voltage transfer efficiency, based on the fact that the induced voltage at the receiving coil increases proportionally with the increase of magnetic flux going though the inductive link.

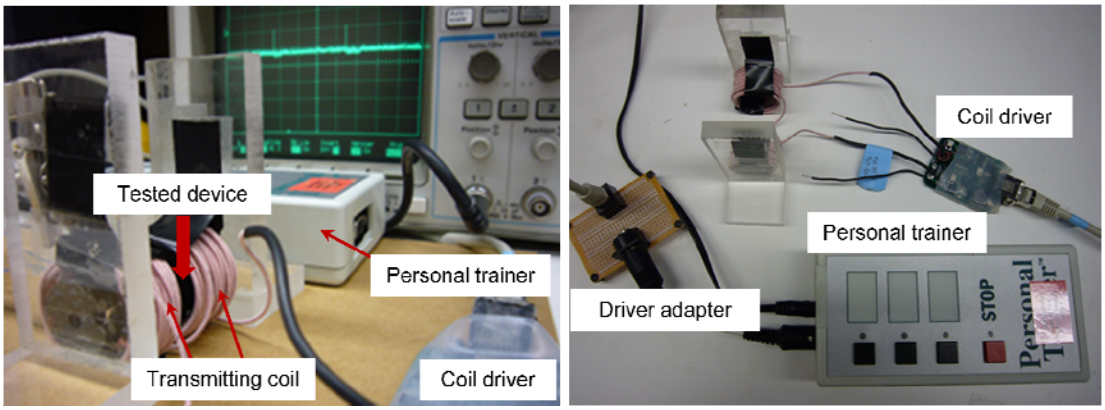


Figure 5.31: A telemetry setup for functionality test of the assembled BION system. The right picture shows a personal trainer and other peripheral accessories.

In vitro measurements have been conducted, and output signals are monitored by connecting two electrodes directly to an HP54645A oscilloscope. Figure 5.32 shows a stimulation pulse recorded from the electrode sites with a pulse width of approximately 500 μs and an amplitude of approximately 7 V. In order to estimate the power transfer capability of the MEMS coil, the voltage across the receiving coil terminals is measured. The current delivered to the chip is also obtained by measuring voltage on an extra resistor in series with the chip. Typical waveforms of the transferred voltage and current are given in Figure 5.33, showing a resonant frequency of ~505 kHz and a ~25 degree phase drift between voltage and current. As mentioned earlier, the tuning capacitor is a commercial chip capacitor, which has limited options of capacitance values. Therefore, it is difficult to fine tune the resonant circuit to achieve precise synchronization.

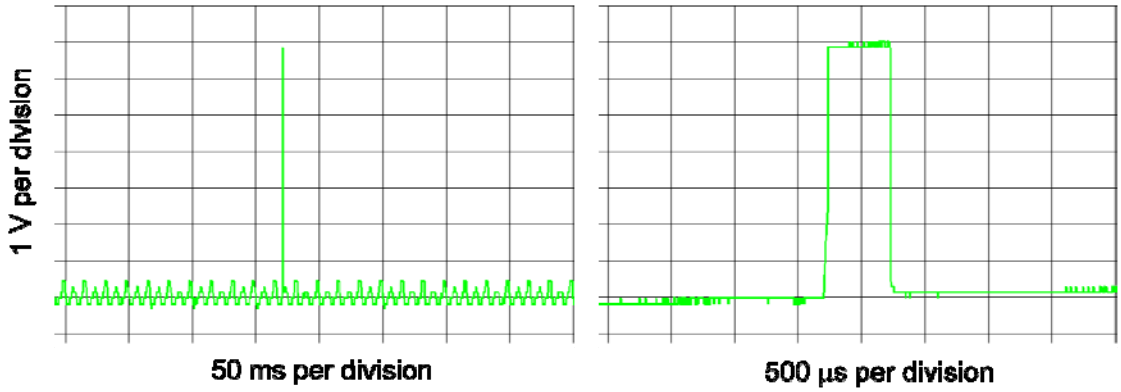


Figure 5.32: Typical simulation pulse measured from the electrode sites.

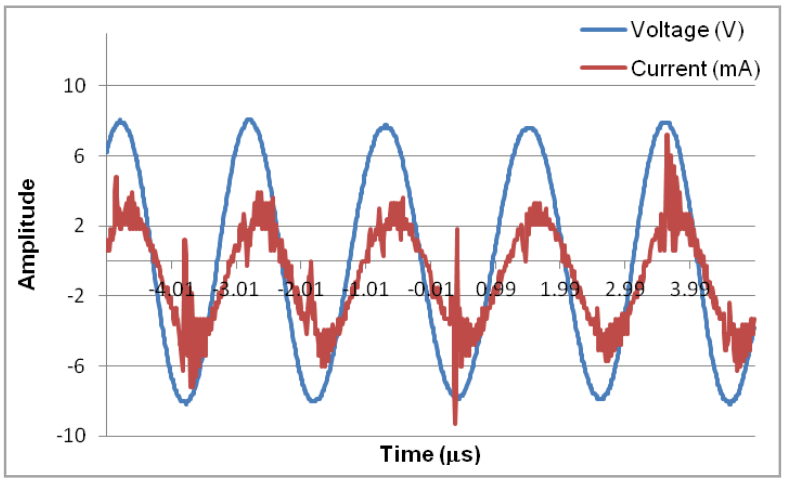


Figure 5.33: Waveforms of transferred voltage and current to the BION circuitry.

The distance between the two coils is varied, and stimulating pulses, transferred voltage as well as delivered power at the different separation distances are recorded and plotted in Figure 5.34. The current system has a detectable range of ~ 4 mm, which is mainly limited by the low Q factor of the receiving coil. The output pulses have amplitudes ranging from ~6.8 V to 8.3 V, depending on the separation distance between the coil pairs. The figure also shows a threshold for the transferred voltage near 7 V, below that no stimulating pulse can be detected from the output electrodes. The maximum power delivered through the inductive link is around 43 mW, and drops dramatically by ~ 62% as

the separation distance increases to 2 mm due to the divergence of the electromagnetic flux at the edge of the primary coil.

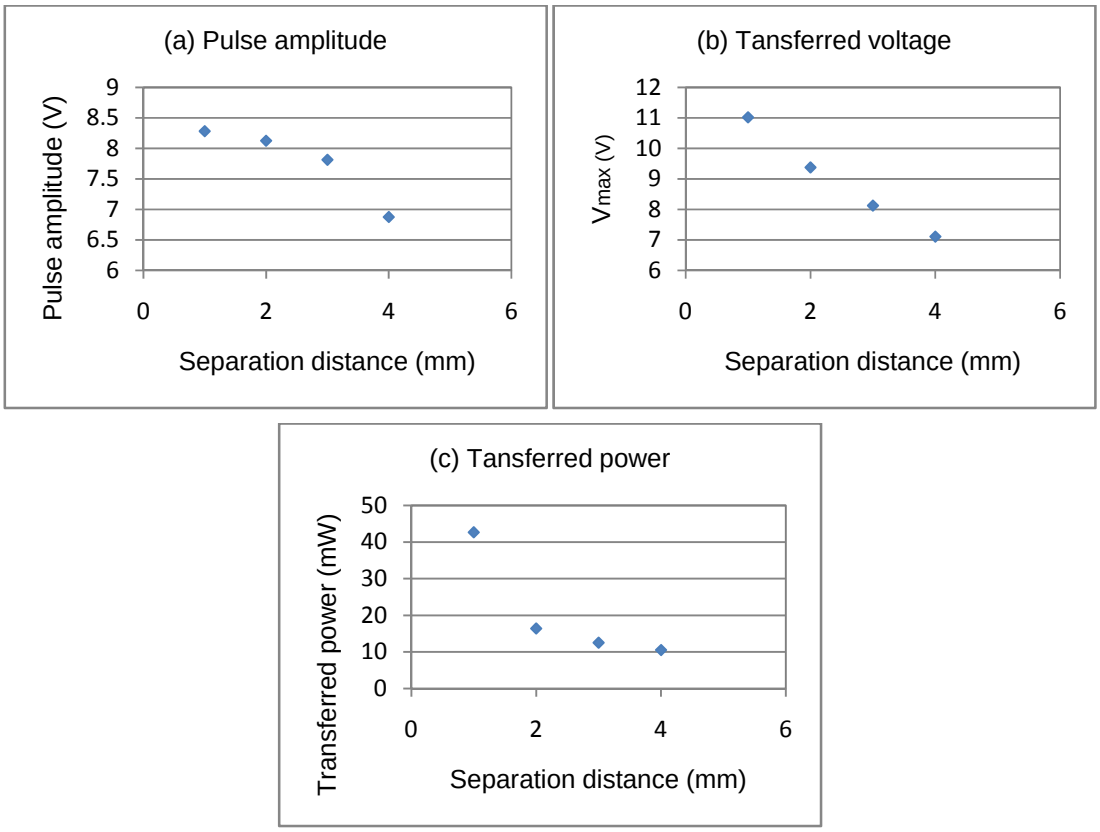


Figure 5.34: Measured stimulating pulses (a), transferred voltages (b) and transferred power (c) at different separation distances between two coils.

5.5.4 **Monolithic system processing**

After demonstrating the functionality of the assemble system, a completely monolithic system is designed and currently undergoing process characterization and refinement, using the BION as the test chip. The complete fabrication process flow is given in Figure 5.35, where the RF coil, platinum 2-electrode array, BION chip and capacitors are integrated in the same platform.

Figure 5.35: Integration process for monolithic neural stimulator.

Because the coil leads are connected to the carrier substrate from the center, a crossover bridge is formed on the overlap area by inserting a layer of sacrificial photoresist and removing it afterwards. One issue associated with this change is that cracks tend to form in the photoresist, and delamination could occur between Parylene and silicon

substrate (Figure 5.36). Some ongoing efforts aim to address these problems and optimize the fabrication processes.

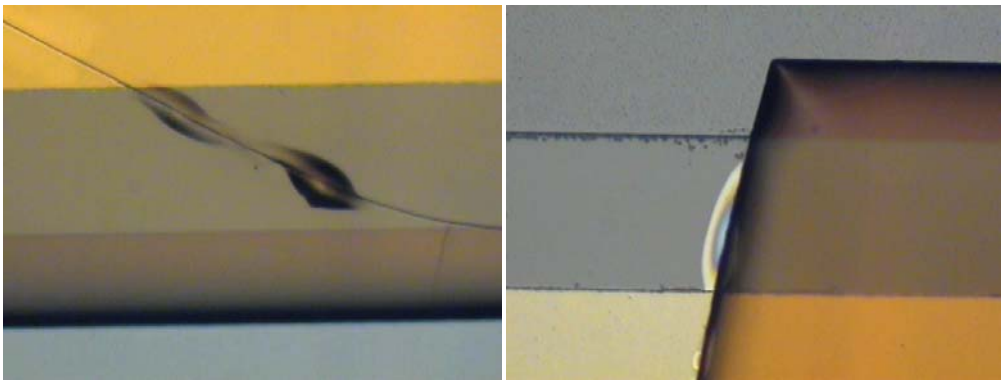


Figure 5.36: Photoresist cracking and Parylene delamination encountered during the monolithic integration processing.

Nevertheless, we have demonstrated our ability to integrate IC circuitry with MEMS components for a fully functional system using the RFID chip. A functional neural stimulator featuring the BION chip has also been implemented. Although a monolithic integrated device has not been fabricated yet, we believe it is just a matter of time. Future work should include finishing the monolithic integration process, and implant the integrated system in animal model to verify its functionality *in vivo*.

5.6 Summary

In this chapter, an embedded chip integration technology has been developed and successfully demonstrated by integrating a flexible Parylene RF coil with a commercially available read-only RFID chip. The functionality of the embedded chip is tested using an RFID reader module. Preliminary accelerated-lifetime passive soak testing has also been done in hot saline, which shows positive results for bioimplant packaging using Parylene. In addition, a neural stimulator, which features a single channel stimulation capability, has

been designed and the first prototype of the integrated system has been fabricated and tested to demonstrate its stimulation function *in vitro*.

APPENDIX A: DUAL-LAYER RF MEMS COIL MICROFABRICATION PROCESS

Substrate: Prime silicon wafers, 550 μm thick, 4 inch diameter. Do not remove native oxide.

I. Alignment mark (Single side):

1) Hexamethyldisilazane (HMDS) primer:
    a. 2mL
    b. Time: 1minute
2) Spin AZ 4400:
    a. Ramp rate: 500 rpm/sec
    b. Spin speed: 4 krpm
    c. Time: 40 seconds
3) Soft bake:
    a. Temperature: 100 °C
    b. Time: 30 minutes
4) Expose in UV cannon:
    a. Time: 20 seconds
5) Develop in AZ 351 developer:
    a. AZ 351: DI water = 1:3
    b. Time: 1 minute 30 seconds
    c. Rinse with DI water
    d. Spin dry
    e. Examine
6) Etch alignment marks in PEII:
    a. Plasma type: SF_6
    b. Plasma pressure/power/time: 200 mTorr/400 W/6 min (rotate wafer every 3 minutes)

II. Optional sacrificial photoresist:

1) HMDS primer:
    a. 2 mL
    b. Time: 1 minute

2) Spin AZ 4400:
    a. Ramp rate: 500 rpm/sec
    b. Spin speed: 4 krpm
    c. Time: 40 seconds
3) Hard bake:
    a. Temperature: 100 °C
    b. Time: over night

III. Deposit Parylene (~ 5 μm):
1) Parylene machine I
2) Parylene C dimer: 7.5 grams

IV. Optional surface treatment of Parylene:
1) PEII plasma roughening:
    a. Plasma type: O_2
    b. Plasma pressure/power/time: 200 mTorr/50 W/1 min
2) Surface cleaning:
    a. Buffered hydrofluoric acid (BHF) cleaning: 20 seconds
    b. Rinse with DI water
    c. Spin dry

V. E-beam metal:
1) Material type: Ti/Au/Ti (Ti optional)
2) Metal thickness: 200 Å /2000 Å /200 Å

VI. Pattern metal:
1) Spin AZ 1518:
    a. Ramp rate: 500 rpm/sec
    b. Spin speed: 3 krpm
    c. Time: 40 seconds
2) Soft bake:
    a. Temperature: 100 °C
    b. Time: 30 minutes
3) Expose in stepper:
    a. Time: 0.35 seconds

4) Develop in AZ 351 developer:
    a. AZ 351: DI water = 1:4
    b. Time: 2 minutes
    c. Rinse with DI water
    d. Spin dry
    e. Examine
5) PEII descum:
    a. Plasma type: O_2
    b. Plasma pressure/power/time: 200 mTorr/50 W/1 min
6) Wet etching:
    a. Ti etchant: BHF ~ 20 seconds
    b. Au etchant: ~ 80 seconds
    c. Rinse with DI water
    d. Spin dry
    e. Examine
7) Strip photoresist:
    a. Solvent: acetone
    b. Time: 5 minutes
    c. Rinse with isopropanol (IPA) and DI water
    d. Spin dry
8) PEII descum:
    a. Plasma type: O_2
    b. Plasma pressure/power/time: 200 mTorr/50 W/ 1 min

VII. Deposit Parylene (insulation layer between two metal layers, ~ 2 μm):

1) Parylene machine I
2) Parylene C dimer: 3 grams

VIII. Etch through vias:

1) Spin AZ 4620:
    a. Ramp rate: 1 krpm/sec
    b. Spin speed: 1 krpm
    c. Time: 40 seconds

2) Soft bake:
    a. Temperature: 100 °C
    b. Time: 30 minutes
3) Expose through via in stepper:
    a. Time: 6 seconds
4) Develop in AZ 351 developer:
    a. AZ 351: DI water = 1:4
    b. Time: 4 minutes
5) Etch Parylene C in RIE:
    a. Plasma type: O_2
    b. Plasma pressure/power/time: 350 mTorr/400 W/8 min (Recipe 3)
6) Strip photoresist in ST-22:
    a. Temperature: 80 °C
    b. Time: 5 minutes
    c. Rinse with post-solvent rinse and DI water
    d. Spin dry
    e. Examine
7) PEII descum:
    a. Plasma type: O_2
    b. Plasma pressure/power/time: 200 mTorr/50 W/1 min

IX. E-beam metal:

1) Material type: Ti /Au /Ti (Ti optional)
3) Metal thickness: 200 Å /2000 Å /200 Å

X. Pattern metal:

1) Spin AZ 4400:
    a. Ramp rate: 500 rpm/sec
    b. Spin speed: 2 krpm
    c. Time: 40 seconds
2) Soft bake:
    a. Temperature: 100 °C
    b. Time: 30 minutes

3) Expose in stepper:
    a. Time: 1.5 seconds
4) Develop in AZ 351 developer:
    a. AZ 351: DI water = 1:4
    b. Time: 4 minutes
    c. Rinse with DI water
    d. Spin dry
    e. Examine
5) PEII descum:
    a. Plasma type: O_2
    b. Plasma pressure/power/time: 200 mTorr/50 W/1 min
6) Wet etching:
    a. Ti etchant: BHF ~ 20 seconds
    b. Au etchant: ~ 80 seconds
    c. Rinse with DI water
    d. Spin dry
    e. Examine
7) Strip photoresist:
    a. Solvent: acetone
    b. Time: 5 minutes
    c. Rinse with IPA and DI water
    d. Spin dry
8) PEII descum:
    a. Plasma type: O_2
    b. Plasma pressure/power/time: 200 mTorr/50 W/1 min

XI. Deposit Parylene (~ 5 μm):

1) Parylene machine I
2) Parylene C dimer: 7.5 grams

XII. Etch Parylene:

1) Spin AZ 9260:
    a. Ramp rate: 1 krpm/sec

b. Spin speed: 1 krpm

c. Time: 40 seconds

2) Soft bake:

a. Temperature: 100 °C

b. Time: 30 minutes

3) Expose in contact aligner:

a. Time: 200 seconds

4) Develop in AZ 351 developer:

a. AZ 351:H2O = 1:3

b. Time: 4 ~ 5 minutes

c. Rinse with DI water

d. Spin dry

e. Examine

XIII. Etch Parylene in RIE:

1) Plasma type: O_2
2) Plasma pressure/power/time: 350 mTorr/400 W/40 min (Recipe 3)
3) Examine

XIV. Release devices:

1) Strip photoresist in acetone
2) Rinse with IPA and DI water
3) Release devices in DI water
4) Oven dry

APPENDIX B: FOLD-AND-BOND RF MEMS COIL MICROFABRICATION PROCESS

Substrate: Prime silicon wafers, 550 μm thick, 4 inch diameter. Do not remove native oxide.

I. Alignment mark (Single side):

1) HMDS primer:
    a. 2mL
    b. Time: 1minute
2) Spin AZ 4400:
    a. Ramp rate: 500 rpm/sec
    b. Spin speed: 4 krpm
    c. Time: 40 seconds
3) Soft bake:
    a. Temperature: 100 °C
    b. Time: 30 minutes
4) Expose in UV cannon:
    a. Time: 20 seconds
5) Develop in AZ 351 developer:
    a. AZ 351: DI water = 1:3
    b. Time: 1 minute 30 seconds
    c. Rinse with DI water
    d. Spin dry
    e. Examine
6) Etch alignment marks in PEII:
    a. Plasma type: SF_6
    b. Plasma pressure/power/time: 200 mTorr/400 W/6 min (rotate wafer every 3 minutes)

II. Optional sacrificial photoresist:

1) HMDS primer:
    a. 2 mL
    b. Time: 1 minute

2) Spin AZ 4400:
    a. Ramp rate: 500 rpm/sec
    b. Spin speed: 4 krpm
    c. Time: 40 seconds
3) Hard bake:
    a. Temperature: 100 °C
    b. Time: over night

III. Deposit Parylene (~ 5 μm):
1) Parylene machine I
2) Parylene C dimer: 7.5 grams

IV. E-beam metal:
1) Material type: Ti/Au/Ti (Ti optional)
2) Metal thickness: 200 Å /2000 Å /200 Å

V. Pattern metal:
1) Spin AZ 1518:
    a. Ramp rate: 500 rpm/sec
    b. Spin speed: 3 krpm
    c. Time: 40 seconds
2) Soft bake:
    a. Temperature: 100 °C
    b. Time: 30 minutes
3) Expose in contact aligner:
    a. Time: 17 seconds
4) Develop in AZ 351 developer:
    a. AZ 351: DI water = 1:4
    b. Time: 1 minutes
    c. Rinse with DI water
    d. Spin dry
    e. Examine
5) PEII descum:
    a. Plasma type: O_2

b. Plasma pressure/power/time: 200 mTorr/50 W/1 min

6) Wet etching:
   a. Ti etchant: BHF ~ 20 seconds
   b. Au etchant: ~ 80 seconds
   c. Rinse with DI water
   d. Spin dry
   e. Examine
7) Strip photoresist:
   a. Solvent: acetone
   b. Time: 5 minutes
   c. Rinse with IPA and DI water
   d. Spin dry
8) PEII descum:
   a. Plasma type: O_2
   b. Plasma pressure/power/time: 200 mTorr/50 W/1 min

VI. Deposit Parylene (~ 5 μm):
1) Parylene machine I
2) Parylene C dimer: 7.5 grams

VII. Etch Parylene:
1) Spin AZ 9260:
   a. Ramp rate: 1 krpm/sec
   b. Spin speed: 1 krpm
   c. Time: 40 seconds
2) Soft bake:
   a. Temperature: 100 °C
   b. Time: 30 minute
3) Expose in contact aligner:
   a. Time: 200 seconds
4) Develop in AZ 351 developer:
   a. AZ351:H2O = 1:3
   b. Time: 4 ~ 5min

c. Rinse with DI water

d. Spin dry

e. Examine

VIII. Etch Parylene in RIE:

1) Plasma type: O_2
2) Plasma pressure/power/time: 350 mTorr/400 W/30 min (Recipe 3)
3) Examine

IX. Release devices:

1) Strip photoresist in acetone
2) Rinse with IPA and DI water
3) Release devices in DI water

X. Thermal bonding and annealing:

1) Align and clamp in the appropriate jig
2) Place in the vacuum oven:
    a. N_2 back fill
    b. Temperature: 220 °C ~ 250 °C
    c. Time: 2 days
3) Vent
4) Examine

APPENDIX C: EMBEDDED CHIP INTEGRATION MICROFABRICATION PROCESS

Substrate: Double-side polished silicon wafers, 550 μm thick, 4 inch diameter. Do not remove native oxide.

I. Double side alignment marks:

1) HMDS primer:
    a. 2 mL
    b. Time: 1 minute
2) Spin AZ 4400 on front side:
    a. Ramp rate: 1 krpm/sec
    b. Spin speed: 4 krpm
    c. Time: 40 seconds
3) Soft bake:
    a. Temperature: 100 °C
    b. Time: 10 minutes
4) Spin AZ 4400 on back side:
    a. Ramp rate: 1 krpm/sec
    b. Spin speed: 4 krpm
    c. Time: 40 seconds
5) Soft bake:
    a. Temperature: 100 °C
    b. Time: 30 minutes
6) Expose in UV cannon:
    a. Time: 20 seconds on each side
7) Develop in AZ 351 developer:
    a. AZ 351: DI water = 1:3
    b. Time: 90 seconds
    c. Rinse in DI H_2O
    d. Spin dry
    e. Examine

8) Etch alignment marks in RIE:
    a. Plasma type: SF_6/O_2
    b. Plasma Pressure/Power/Time: 120 mTorr/120 W/10 min (Recipe 4)
9) Strip photoresist in ST-22:
    a. Temperature: 80 °C
    b. Time: ~ 10 minutes
    c. Rinse in post-solvent rinse and DI water
    d. Spin dry
    e. Examine

II. Etch Parylene anchors:

1) HMDS primer:
    a. 2 mL
    b. Time: 1 minute
2) Spin AZ 4400:
    a. Ramp rate: 500 rpm/sec
    b. Spin speed: 4 krpm
    c. Time: 40 seconds
3) Soft bake:
    a. Temperature: 100 °C
    b. Time: 30 minutes
4) Expose in stepper:
    a. Time: 1.5 seconds
5) Develop in AZ 351 developer:
    a. AZ 351: DI water = 1:4
    b. Time: 90 seconds
    c. Rinse with DI water
    d. Spin dry
    e. Examine
6) PEII Descum:
    a. Plasma type: O_2
    b. Plasma pressure/power/time: 200mTorr/50W/1min

7) BHF cleaning:
    a. 20 seconds
    b. Rinse with DI water
    c. Spin dry
8) Etch anchor in DRIE
9) Examine
10) Do not remove photoresist:
    a. Hard bake: over night

III. Deposit Parylene (~5 μm):
1) Protect back side with black tapes
2) Parylene machine I
3) Parylene C dimer: 7.5 grams

IV. E-beam metal:
1) Material type: Au
2) Metal thickness: 5000 Å

V. Pattern metal:
1) Spin AZ 1518:
    a. Ramp rate: 500 rpm/sec
    b. Spin speed: 3 krpm
    c. Time: 40 seconds
2) Soft bake:
    a. Temperature: 100 °C
    b. Time: 30 minutes
4) Expose in contact aligner:
    a. Time: 17 seconds
5) Develop in AZ 351 developer:
    a. AZ 351: DI water = 1:4
    b. Time: 1 minutes
    c. Rinse with DI water
    d. Spin dry
    e. Examine

6) PEII descum:
    a. Plasma type: O_2
    b. Plasma pressure/power/time: 200mTorr/50W/1min
7) Au etching:
    a. Time: 150 seconds
    b. Rinse with DI water
    c. Spin dry
    d. Examine
8) Strip photoresist:
    a. Solvent: acetone
    b. Time: 5 minutes
    c. Rinse with IPA and DI water
    d. Spin dry
    e. Examine
9) PEII descum:
    a. Plasma type: O_2
    b. Plasma pressure/power/time: 200mTorr/50W/1min

VI. Etch chip cavities:

1) Spin AZ 9260:
    a. Ramp rate: 1 krpm/sec
    b. Spin speed: 1 krpm
    c. Time: 40 seconds,
2) Soft bake:
    a. Temperature: 100 °C
    b. Time: 30 minutes
3) Expose in contact aligner:
    a. Time: 200 seconds
4) Develop in AZ 351 developer:
    a. AZ 351: DI water = 1:3
    b. Time: 4~5 minutes
    c. Rinse with DI water

a. Spin dry

b. Examine

5) Etch Parylene in RIE:

a. Plasma type: O_2

b. Plasma pressure/power/time: 350 mTorr/400 W/15 min (Recipe 3)

c. Examine

6) Strip photoresist:

a. Solvent: acetone

b. Time: 5 minutes

c. Rinse with IPA and DI water

d. Spin dry

e. Examine

7) Spin AZ 9260:

a. Ramp rate: 1 krpm/sec

b. Spin speed: 1 krpm

c. Time: 40 seconds

8) Soft bake:

a. Temperature: 100 °C

b. Time: 30 minutes

9) Expose in contact aligner:

a. Time: 200 seconds

10) Develop in AZ 351 developer:

a. AZ 351: DI water = 1:3

b. Time: 4~5 minutes

c. Rinse with DI water

a. Spin dry

b. Examine

11) Remove photoresist edge

12) PEII descum:

a. Plasma type: O_2

b. Plasma pressure/power/time: 200mTorr/50W/1min

13) Hard bake:
    a. Time: over night
14) BHF cleaning:
    a. Time: 20 seconds
    b. Rinse with DI water
    c. Spin dry
15) Etch chip cavity in DRIE:
    a. Bosch process: B=7 seconds
    b. 300 loops
    c. Examine, and measured depth in WYKO
16) Strip photoresist:
    a. Solvent: acetone
    b. Time: 5 minutes
    c. Rinse with IPA and DI water
    d. Spin dry
    e. Examine
17) PEII descum:
    a. Plasma type: O_2
    b. Plasma pressure/power/time: 200mTorr/50W/1min

VII. Drop chips into cavities:

1) drop 5-minute epoxy into cavities
2) Align chips in cavities
3) Flatten wafer surface
4) Cure epoxy at room temperature

VIII. Deposit Parylene (~2 μm):

1) Protect back side with black tapes
2) Parylene machine I
3) Parylene C dimer: 3 grams

IX. Etch through vias:

1) Spin AZ 9260:
    a. Ramp rate: 1 krpm/sec

b. Spin speed: 1 krpm

c. Time: 40 seconds

2) Soft bake:

a. Temperature: 100 °C

b. Time: 30 minutes

3) Expose through via in contact aligner:

a. Time: 200 seconds

4) Develop in AZ 351 developer

a. AZ 351: DI water = 1:3

b. Time: 4~5 minutes

5) Etch Parylene C in RIE

a. Plasma type: O_2

b. Plasma pressure/power/time: 350 mTorr/400 W/8 min (Recipe 3)

6) Strip photoresist

a. Solvent: acetone

b. Time: 5 minutes

c. Rinse with IPA and DI water

d. Spin dry

e. Examine

7) PEII descum:

a. Plasma type: O_2

b. Plasma pressure/power/time: 200 mTorr/50 W/1 min

X. E-beam metal:

1) Material type: Au

2) Metal thickness: 5000 Å

XI. Pattern metal:

1) Spin AZ 9620:

a. Ramp rate: 1 krpm/sec

b. Spin speed: 1 krpm

c. Time: 40 seconds

2) Soft bake:

a. Temperature: 100 °C

b. Time: 30 minutes

10) Expose in contact aligner:

a. Time: 200 seconds

11) Develop in AZ 351 developer:

a. AZ 351: DI water = 1:3

b. Time: 4~5 minutes

c. Rinse with DI water

d. Spin dry

e. Examine

12) PEII descum:

c. Plasma type: O_2

d. Plasma pressure/power/time: 200mTorr/50W/1min

13) Au etching:

a. Time: 150 seconds

b. Rinse with DI water

c. Spin dry

d. Examine

14) Strip photoresist:

a. Solvent: acetone

b. Time: 5 minutes

c. Rinse with IPA and DI water

d. Spin dry

e. Examine

15) PEII descum:

a. Plasma type: O_2

b. Plasma pressure/power/time: 200mTorr/50W/1min

XII. Deposit Parylene (~5um):

1) Protect back side with black tapes

2) Parylene machine I

3) Parylene C dimer: 7.5 grams

XIII. Etch Parylene:

1) Spin AZ 9260:
    a. Ramp rate: 1 krpm/sec
    b. Spin speed: 1 krpm
    c. Time: 40 seconds
2) Soft bake:
    a. Temperature: 100 °C
    b. Time: 30 minutes
3) Expose in contact aligner:
    a. Time: 200 seconds
4) Develop in AZ 351 developer:
    a. AZ 351: DI water = 1:3
    b. Time: 4~5 minutes
    c. Rinse in DI water
    d. Examine
5) Etch Parylene C in RIE:
    a. Plasma type: O_2
    b. Plasma pressure/power/time: 350 mTorr/400 W/40 min (Recipe 3)
6) Strip photoresist:
    a. Solvent: acetone
    b. Time: 5 minutes
    c. Rinse with IPA and DI water
    d. Spin dry
    e. Examine

XIV. Etch through Si from the back side:

1) Spin AZ 9260 on the front side:
    a. Ramp rate: 1 krpm/sec
    b. Spin speed: 1 krpm
    c. Time: 40 seconds
2) Soft bake:
    a. Temperature: 100 °C

b. Time: 30 minutes

3) Spin AZ 9260 on the back side:
    a. Ramp rate: 1 krpm/sec
    b. Spin speed: 1 krpm
    c. Time: 40 seconds
4) Soft bake:
    a. Temperature: 100 °C
    b. Time: 30 minutes
5) Expose in contact aligner:
    a. Time: 200 seconds
6) Develop in AZ 351 developer:
    a. AZ 351: DI water = 1:3
    b. Time: 4~5 minutes
    c. Rinse in DI water
    d. Spin dry
    e. Examine
7) Remove photoresist edge on the back side
8) PEII descum:
    a. Plasma type: O_2
    b. Plasma pressure/power/time: 200 mTorr/50 W/1 min
9) Spin AZ 4400 on backing wafer:
    a. Ramp rate: 500 rpm/sec
    b. Spin speed: 2 krpm
    c. Time: 40 seconds
10) Stack the processed wafer on backing wafer
11) Hard bake:
    a. Temperature: 100 °C
    b. Time: over night
12) BHF cleaning:
    a. Time: 20 seconds
13) Etch Si in DRIE:

a. Bosch process: B = 7 seconds

b. 760 loops

c. Examine

XV. Release device in acetone:

1) Time: over night
2) Rinse with IPA and DI water
3) Oven dry

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